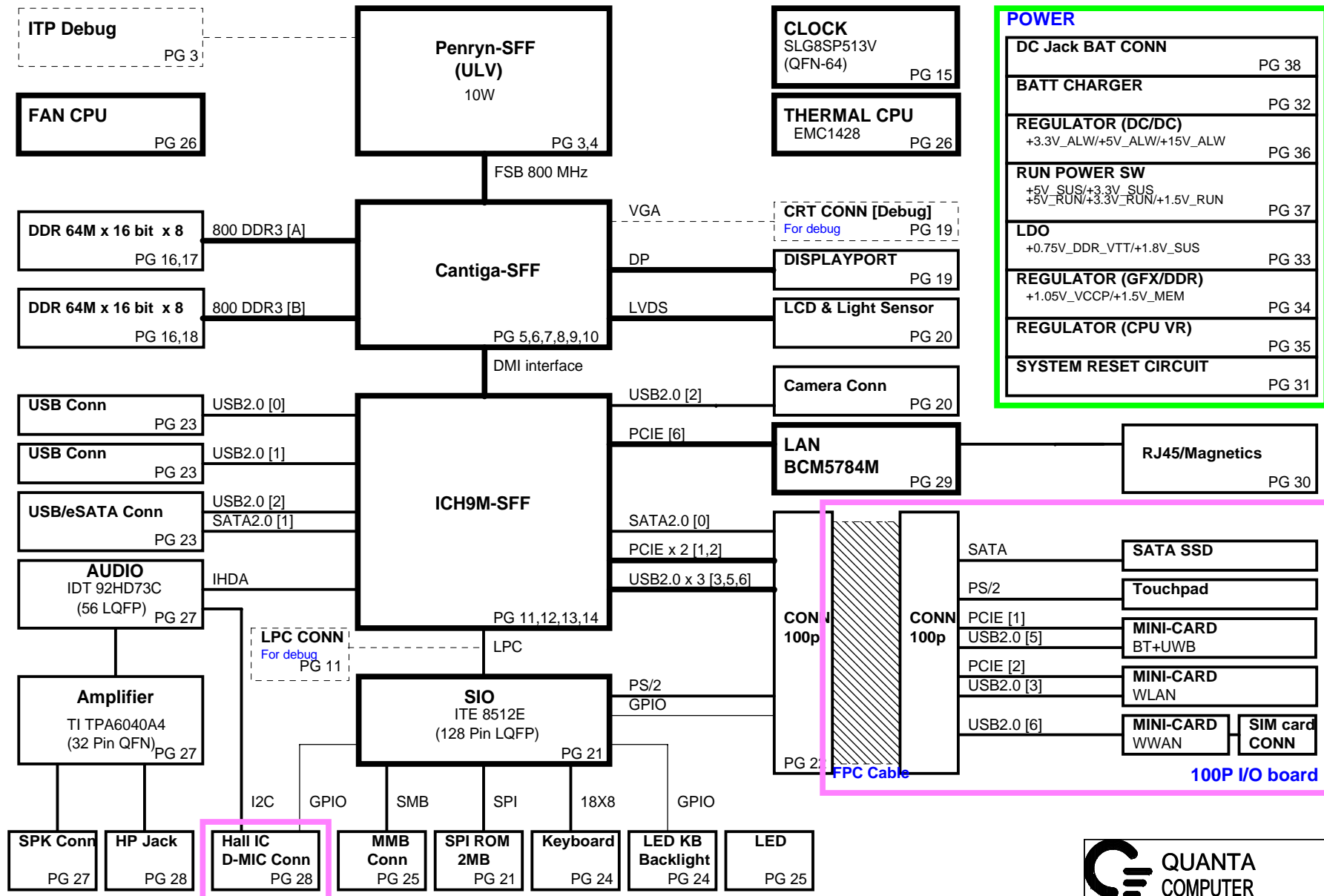



Rev: A00

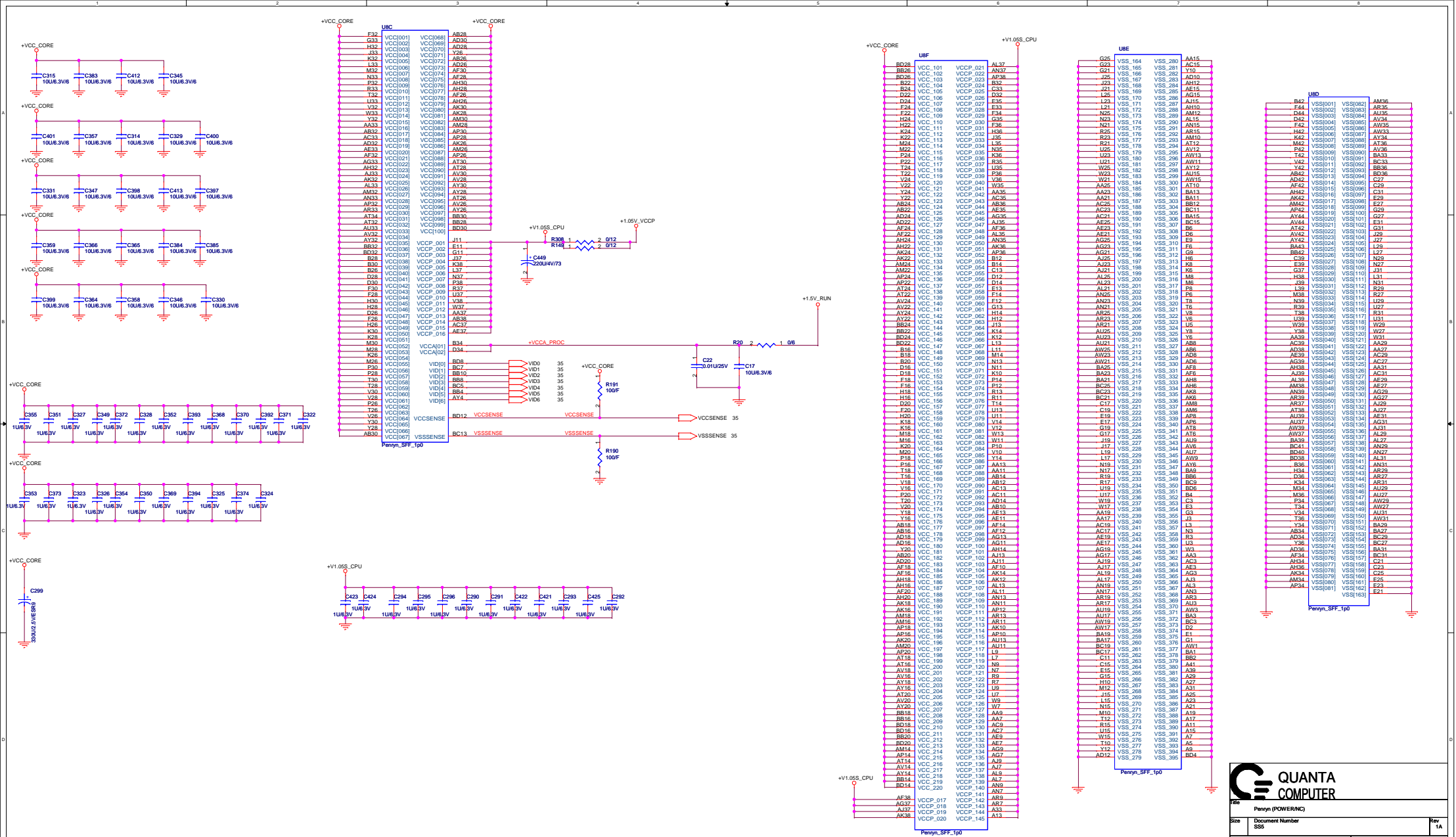


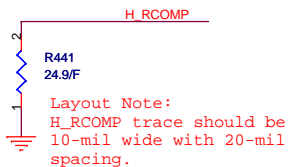
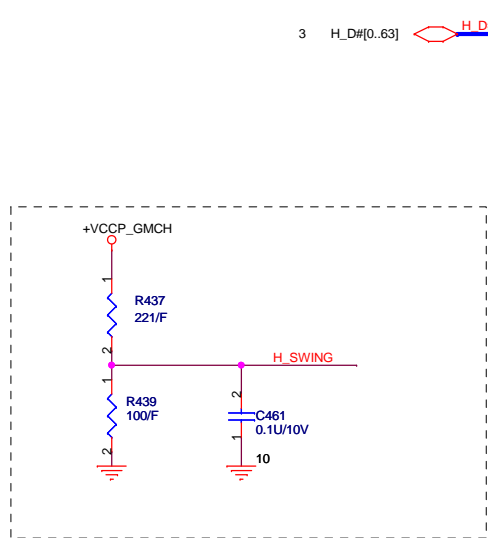
1	2	3	4	5	6	7	8
A							
B							
C							
D							



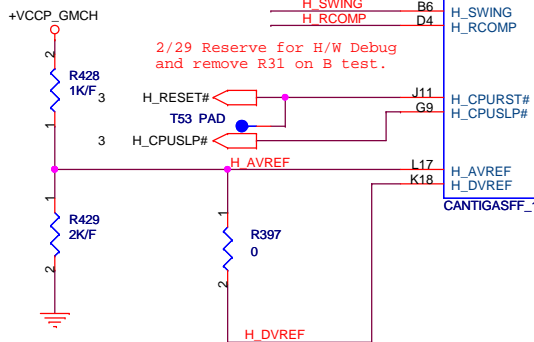
QUANTA
COMPUTER

Title		
Index & Power Status		
Size	Document Number	Rev
SS5		1A
Date:	Thursday, January 08, 2009	Sheet 2 of 44





Layout Note:
H_RCOMP trace should be
10-mil wide with 20-mil
spacing.



2/29 Reserve for H/W Debug
and remove R31 on B test.

H_RESET#
T53 PAD
H_CPUSLP#

H_AVREF

H_DVREF

U6A

H_D#0 J7 H_D#_0
H_D#1 J6 H_D#_1
H_D#2 L11 H_D#_2
H_D#3 J3 H_D#_3
H_D#4 H4 H_D#_4
H_D#5 G3 H_D#_5
H_D#6 K10 H_D#_6
H_D#7 K12 H_D#_7
H_D#8 L1 H_D#_8
H_D#9 M10 H_D#_9
H_D#10 M6 H_D#_10
H_D#11 N11 H_D#_11
H_D#12 L7 H_D#_12
H_D#13 K6 H_D#_13
H_D#14 M4 H_D#_14
H_D#15 K4 H_D#_15
H_D#16 P6 H_D#_16
H_D#17 W9 H_D#_17
H_D#18 V6 H_D#_18
H_D#19 V2 H_D#_19
H_D#20 P10 H_D#_20
H_D#21 W7 H_D#_21
H_D#22 N9 H_D#_22
H_D#23 P4 H_D#_23
H_D#24 U9 H_D#_24
H_D#25 V4 H_D#_25
H_D#26 U1 H_D#_26
H_D#27 W3 H_D#_27
H_D#28 V10 H_D#_28
H_D#29 U7 H_D#_29
H_D#30 W11 H_D#_30
H_D#31 U11 H_D#_31
H_D#32 AC11 H_D#_32
H_D#33 AC9 H_D#_33
H_D#34 Y4 H_D#_34
H_D#35 Y10 H_D#_35
H_D#36 AB6 H_D#_36
H_D#37 AA9 H_D#_37
H_D#38 AB10 H_D#_38
H_D#39 AA1 H_D#_39
H_D#40 AC3 H_D#_40
H_D#41 AC7 H_D#_41
H_D#42 AD12 H_D#_42
H_D#43 AB4 H_D#_43
H_D#44 Y6 H_D#_44
H_D#45 AD10 H_D#_45
H_D#46 AD11 H_D#_46
H_D#47 AB2 H_D#_47
H_D#48 AD4 H_D#_48
H_D#49 AE7 H_D#_49
H_D#50 AD2 H_D#_50
H_D#51 AD6 H_D#_51
H_D#52 AE3 H_D#_52
H_D#53 AG9 H_D#_53
H_D#54 AG7 H_D#_54
H_D#55 AE11 H_D#_55
H_D#56 AK6 H_D#_56
H_D#57 AF6 H_D#_57
H_D#58 AJ9 H_D#_58
H_D#59 AH6 H_D#_59
H_D#60 AF12 H_D#_60
H_D#61 AH4 H_D#_61
H_D#62 AJ7 H_D#_62
H_D#63 AE9 H_D#_63

HOST

H_ADS#
H_ADSTB#_0
H_ADSTB#_1
H_BNR#
H_BPR#
H_BREQ#
H_DEFER#
H_DBSY#
HPLL_CLK
HPLL_CLK#
H_DPWR#
H_DRDY#
H_HIT#
H_HITM#
H_LOCK#
H_TRDY#

H_DINV#_0
H_DINV#_1
H_DINV#_2
H_DINV#_3

H_DSTBN#_0
H_DSTBN#_1
H_DSTBN#_2
H_DSTBN#_3

H_DSTBP#_0
H_DSTBP#_1
H_DSTBP#_2
H_DSTBP#_3

H_REQ#_0
H_REQ#_1
H_REQ#_2
H_REQ#_3
H_REQ#_4

H_RS#_0
H_RS#_1
H_RS#_2

H_A#_3 L15 H_A#3
H_A#_4 B14 H_A#4
H_A#_5 C15 H_A#5
H_A#_6 D12 H_A#6
H_A#_7 F14 H_A#7
H_A#_8 G17 H_A#8
H_A#_9 B12 H_A#9
H_A#_10 J15 H_A#10
H_A#_11 D16 H_A#11
H_A#_12 C17 H_A#12
H_A#_13 D14 H_A#13
H_A#_14 K16 H_A#14
H_A#_15 F16 H_A#15
H_A#_16 C21 H_A#16
H_A#_17 D18 H_A#17
H_A#_18 J19 H_A#18
H_A#_19 J21 H_A#19
H_A#_20 B18 H_A#20
H_A#_21 D22 H_A#21
H_A#_22 G19 H_A#22
H_A#_23 J17 H_A#23
H_A#_24 L21 H_A#24
H_A#_25 C21 H_A#25
H_A#_26 G21 H_A#26
H_A#_27 D20 H_A#27
H_A#_28 K22 H_A#28
H_A#_29 F18 H_A#29
H_A#_30 K20 H_A#30
H_A#_31 F20 H_A#31
H_A#_32 F22 H_A#32
H_A#_33 B20 H_A#33
H_A#_34 A19 H_A#34
H_A#_35

H_ADS#
H_ADSTB#_0
H_ADSTB#_1
H_BNR#
H_BPR#
H_BREQ#
H_DEFER#
H_DBSY#
HPLL_CLK
HPLL_CLK#
H_DPWR#
H_DRDY#
H_HIT#
H_HITM#
H_LOCK#
H_TRDY#

H_DINV#_0
H_DINV#_1
H_DINV#_2
H_DINV#_3

H_DSTBN#_0
H_DSTBN#_1
H_DSTBN#_2
H_DSTBN#_3

H_DSTBP#_0
H_DSTBP#_1
H_DSTBP#_2
H_DSTBP#_3

H_REQ#_0
H_REQ#_1
H_REQ#_2
H_REQ#_3
H_REQ#_4

H_RS#_0
H_RS#_1
H_RS#_2

H_ADS# 3
H_ADSTB#0 3
H_ADSTB#1 3
H_BNR# 3
H_BPR# 3
H_BREQ# 3
H_DEFER# 3
H_DBSY# 3
CLK_MCH_BCLK 15
CLK_MCH_BCLK# 15
H_DPWR# 3
H_DRDY# 3
H_HIT# 3
H_HITM# 3
H_LOCK# 3
H_TRDY# 3

H_DINV#0 3
H_DINV#1 3
H_DINV#2 3
H_DINV#3 3

H_DSTBN#0 3
H_DSTBN#1 3
H_DSTBN#2 3
H_DSTBN#3 3

H_DSTBP#0 3
H_DSTBP#1 3
H_DSTBP#2 3
H_DSTBP#3 3

H_REQ#0 3
H_REQ#1 3
H_REQ#2 3
H_REQ#3 3
H_REQ#4 3

H_RS#0 3
H_RS#1 3
H_RS#2 3



Title
Cantiga_A (HOST)

Size
Custom

Document Number
SS5

Date: Thursday, January 08, 2009

Sheet 5 of 44

Rev
1A



44

17 DDR_A_D[0..63]

DDR A D0 AP46
DDR A D1 AU47
DDR A D2 AT46
DDR A D3 AU49
DDR A D4 AR45
DDR A D5 AN49
DDR A D6 AV50
DDR A D7 AP50
DDR A D8 AW47
DDR A D9 BD50
DDR A D10 AW49
DDR A D11 BA49
DDR A D12 BC49
DDR A D13 AV46
DDR A D14 BA47
DDR A D15 AY50
DDR A D16 BF46
DDR A D17 BC47
DDR A D18 BF50
DDR A D19 BF48
DDR A D20 BC43
DDR A D21 BE49
DDR A D22 BA43
DDR A D23 BE47
DDR A D24 BF42
DDR A D25 BC39
DDR A D26 BF44
DDR A D27 BF40
DDR A D28 BB40
DDR A D29 BE43
DDR A D30 BF38
DDR A D31 BE41
DDR A D32 BA15
DDR A D33 BE11
DDR A D34 BE15
DDR A D35 BE14
DDR A D36 BB14
DDR A D37 BC15
DDR A D38 BE13
DDR A D39 BF16
DDR A D40 BF10
DDR A D41 BC11
DDR A D42 BF8
DDR A D43 BC7
DDR A D44 BC7
DDR A D45 BC9
DDR A D46 BD6
DDR A D47 BF12
DDR A D48 AV6
DDR A D49 BB6
DDR A D50 AW7
DDR A D51 AY6
DDR A D52 AT10
DDR A D53 AW11
DDR A D54 AU11
DDR A D55 AW9
DDR A D56 AR11
DDR A D57 AT6
DDR A D58 AP6
DDR A D59 AL7
DDR A D60 AR7
DDR A D61 AT12
DDR A D62 AM6
DDR A D63 AU7

U6D

DDR SYSTEM MEMORY A

SA_BS_0
SA_BS_1
SA_BS_2

SA_RAS#
SA_CAS#
SA_WE#

SA_DM_0
SA_DM_1
SA_DM_2
SA_DM_3
SA_DM_4
SA_DM_5
SA_DM_6
SA_DM_7

SA_DQS_0
SA_DQS_1
SA_DQS_2
SA_DQS_3
SA_DQS_4
SA_DQS_5
SA_DQS_6
SA_DQS_7
SA_DQS#_0
SA_DQS#_1
SA_DQS#_2
SA_DQS#_3
SA_DQS#_4
SA_DQS#_5
SA_DQS#_6
SA_DQS#_7

SA_MA_0
SA_MA_1
SA_MA_2
SA_MA_3
SA_MA_4
SA_MA_5
SA_MA_6
SA_MA_7
SA_MA_8
SA_MA_9
SA_MA_10
SA_MA_11
SA_MA_12
SA_MA_13
SA_MA_14

BC21 DDR A BS0
BJ21 DDR A BS1
BJ41 DDR A BS2

BH22 DDR A CAS#
BK20 DDR A RAS#
BL15 DDR A WE#

AT50 DDR A DM0
BB50 DDR A DM1
BB46 DDR A DM2
BE39 DDR A DM3
BB12 DDR A DM4
BE7 DDR A DM5
AV10 DDR A DM6
AR9 DDR A DM7

AR47 DDR A DQS0
BA45 DDR A DQS1
BE45 DDR A DQS2
BC41 DDR A DQS3
BC13 DDR A DQS4
BB10 DDR A DQS5
BA7 DDR A DQS6
AN7 DDR A DQS7
AR49 DDR A DQS#0
AW45 DDR A DQS#1
BC45 DDR A DQS#2
BA41 DDR A DQS#3
BA13 DDR A DQS#4
BA11 DDR A DQS#5
BA9 DDR A DQS#6
AN9 DDR A DQS#7

BC23 DDR A MA0
BF22 DDR A MA1
BE31 DDR A MA2
BC31 DDR A MA3
BH26 DDR A MA4
BJ35 DDR A MA6
BB34 DDR A MA7
BH32 DDR A MA8
BB26 DDR A MA9
BF32 DDR A MA10
BA21 DDR A MA11
BG25 DDR A MA12
BH34 DDR A MA13
BH18 DDR A MA14
BE25 DDR A MA14

18 DDR_B_D[0..63]

DDR B D0 AP54
DDR B D1 AM52
DDR B D2 AR55
DDR B D3 AV54
DDR B D4 AM54
DDR B D5 AN53
DDR B D6 AT52
DDR B D7 AU53
DDR B D8 AW53
DDR B D9 AY52
DDR B D10 BB52
DDR B D11 BC53
DDR B D12 AV52
DDR B D13 AW55
DDR B D14 BD52
DDR B D15 BC55
DDR B D16 BE54
DDR B D17 BE51
DDR B D18 BH48
DDR B D19 BK48
DDR B D20 BE53
DDR B D21 BH52
DDR B D22 BK46
DDR B D23 BJ47
DDR B D24 BJ45
DDR B D25 BJ45
DDR B D26 BL41
DDR B D27 BH44
DDR B D28 BH46
DDR B D29 BK44
DDR B D30 BK40
DDR B D31 BJ39
DDR B D32 BK10
DDR B D33 BH10
DDR B D34 BK6
DDR B D35 BH6
DDR B D36 BJ9
DDR B D37 BL11
DDR B D38 BG5
DDR B D39 BJ5
DDR B D40 BG3
DDR B D41 BF4
DDR B D42 BD4
DDR B D43 BA3
DDR B D44 BE5
DDR B D45 BE2
DDR B D46 BB4
DDR B D47 AY4
DDR B D48 BA1
DDR B D49 AP2
DDR B D50 AU1
DDR B D51 AT2
DDR B D52 AT4
DDR B D53 AV4
DDR B D54 AU3
DDR B D55 AR3
DDR B D56 AN1
DDR B D57 AP4
DDR B D58 AL3
DDR B D59 AJ1
DDR B D60 AK4
DDR B D61 AM4
DDR B D62 AH2
DDR B D63 AK2

U6E

DDR SYSTEM MEMORY B

SB_BS_0
SB_BS_1
SB_BS_2

SB_RAS#
SB_CAS#
SB_WE#

SB_DM_0
SB_DM_1
SB_DM_2
SB_DM_3
SB_DM_4
SB_DM_5
SB_DM_6
SB_DM_7

SB_DQS_0
SB_DQS_1
SB_DQS_2
SB_DQS_3
SB_DQS_4
SB_DQS_5
SB_DQS_6
SB_DQS_7
SB_DQS#_0
SB_DQS#_1
SB_DQS#_2
SB_DQS#_3
SB_DQS#_4
SB_DQS#_5
SB_DQS#_6
SB_DQS#_7

SB_MA_0
SB_MA_1
SB_MA_2
SB_MA_3
SB_MA_4
SB_MA_5
SB_MA_6
SB_MA_7
SB_MA_8
SB_MA_9
SB_MA_10
SB_MA_11
SB_MA_12
SB_MA_13
SB_MA_14

BJ13 DDR B BS0
BK12 DDR B BS1
BK38 DDR B BS2

BE21 DDR B CAS#
BH14 DDR B RAS#
BK14 DDR B WE#

AP52 DDR B DM0
AY54 DDR B DM1
BJ49 DDR B DM2
BJ43 DDR B DM3
BH12 DDR B DM4
BD2 DDR B DM5
AY2 DDR B DM6
AJ3 DDR B DM7

AR53 DDR B DQS0
BA53 DDR B DQS1
BH50 DDR B DQS2
BK42 DDR B DQS3
BH8 DDR B DQS4
BH2 DDR B DQS5
AV2 DDR B DQS6
AM2 DDR B DQS7
AT54 DDR B DQS#0
BB54 DDR B DQS#1
BJ51 DDR B DQS#2
BH42 DDR B DQS#3
BK8 DDR B DQS#4
BC3 DDR B DQS#5
AW3 DDR B DQS#6
AN3 DDR B DQS#7

BJ15 DDR B MA0
BJ33 DDR B MA1
BH24 DDR B MA2
BA17 DDR B MA3
BE36 DDR B MA5
BH38 DDR B MA6
BK34 DDR B MA7
BJ37 DDR B MA8
BH40 DDR B MA9
BH16 DDR B MA10
BK36 DDR B MA11
BH38 DDR B MA12
BJ11 DDR B MA13
BL37 DDR B MA14

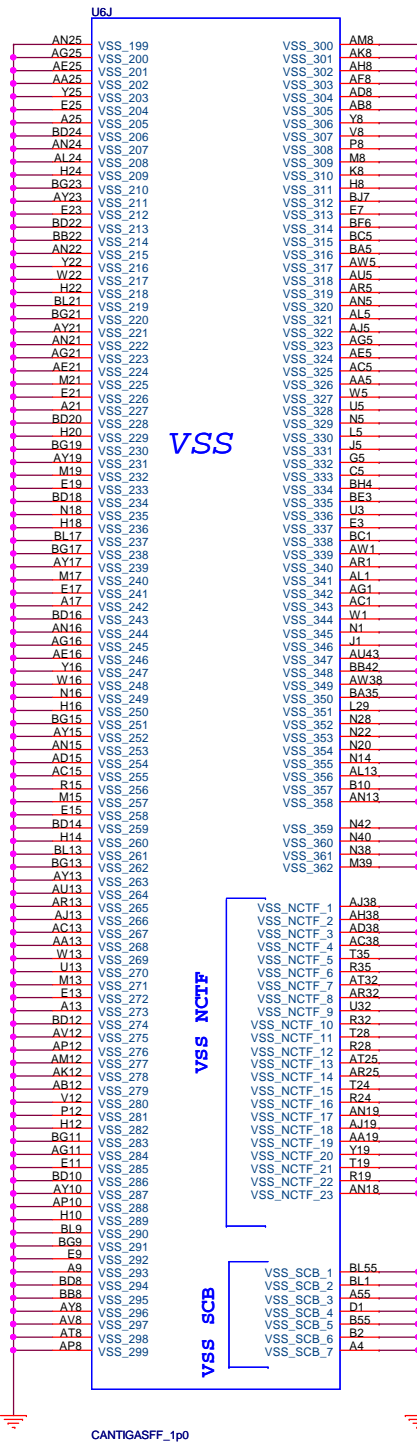
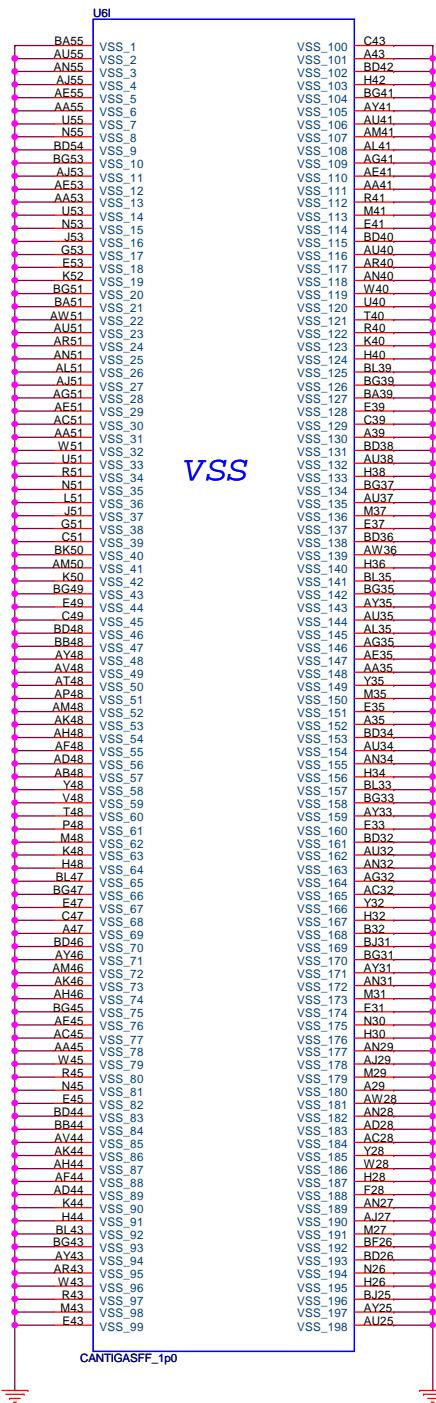
CANTIGASFF_1p0

CANTIGASFF_1p0



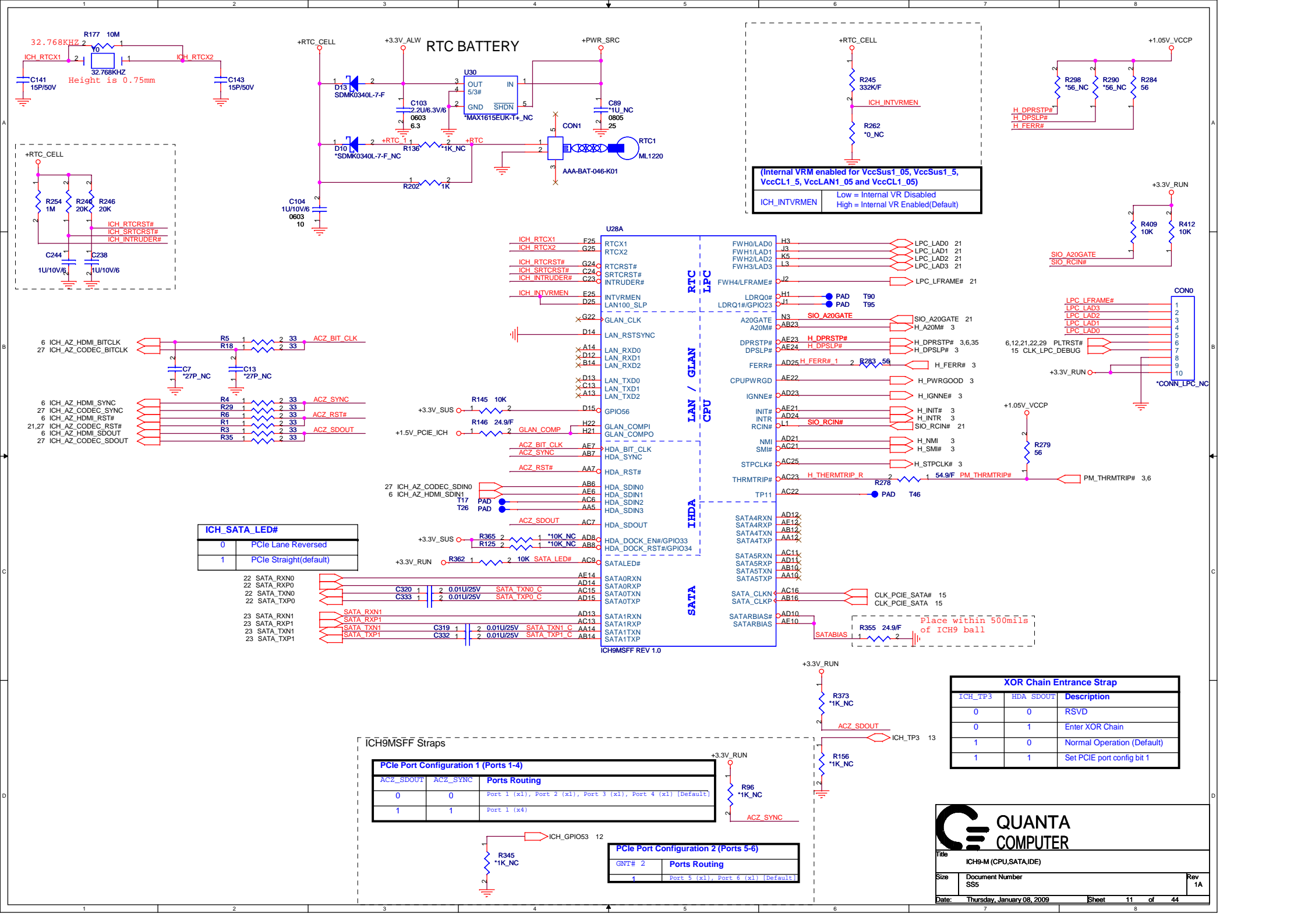
QUANTA
COMPUTER

Title Cantiga_C (DDR3)		
Size	Document Number SS5	Rev 1A
Date: Thursday, January 08, 2009 Sheet 7 of 44		



QUANTA
COMPUTER

File Cantiga_F (VSS)		
Size SS5	Document Number SS5	Rev 1A
Date Thursday, January 08, 2009	Sheet 10	of 44



Place TX DC blocking caps close ICH9.

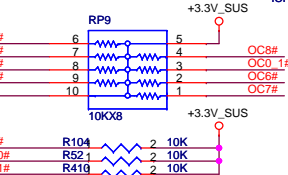
BT & UWB

WLAN

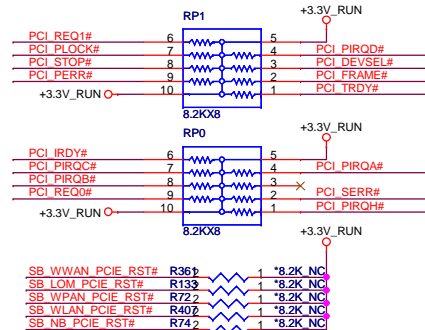
Giga Bit LOM

Boot BIOS Strap			
	GNT0#	SPI_CS1#	
LPC	11	No stuff	No stuff
PCI	10	No stuff	Stuff
SPI	01	Stuff	No stuff

Short F2 and F3 at the package and keep length to less than 500mils. Trace Impedance should be 60ohms +/- 15%.



PCI Pullups



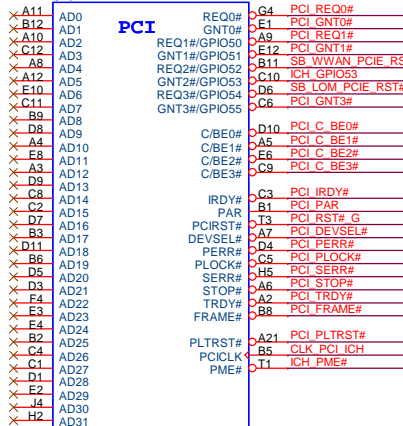
BIOS should not enable the internal GPIO pull up resistor.

A16 away override strap.

PCI_GNT#3 Low = A16 swap override enabled. High = Default.

U28B

PCI



Interrupt I/F

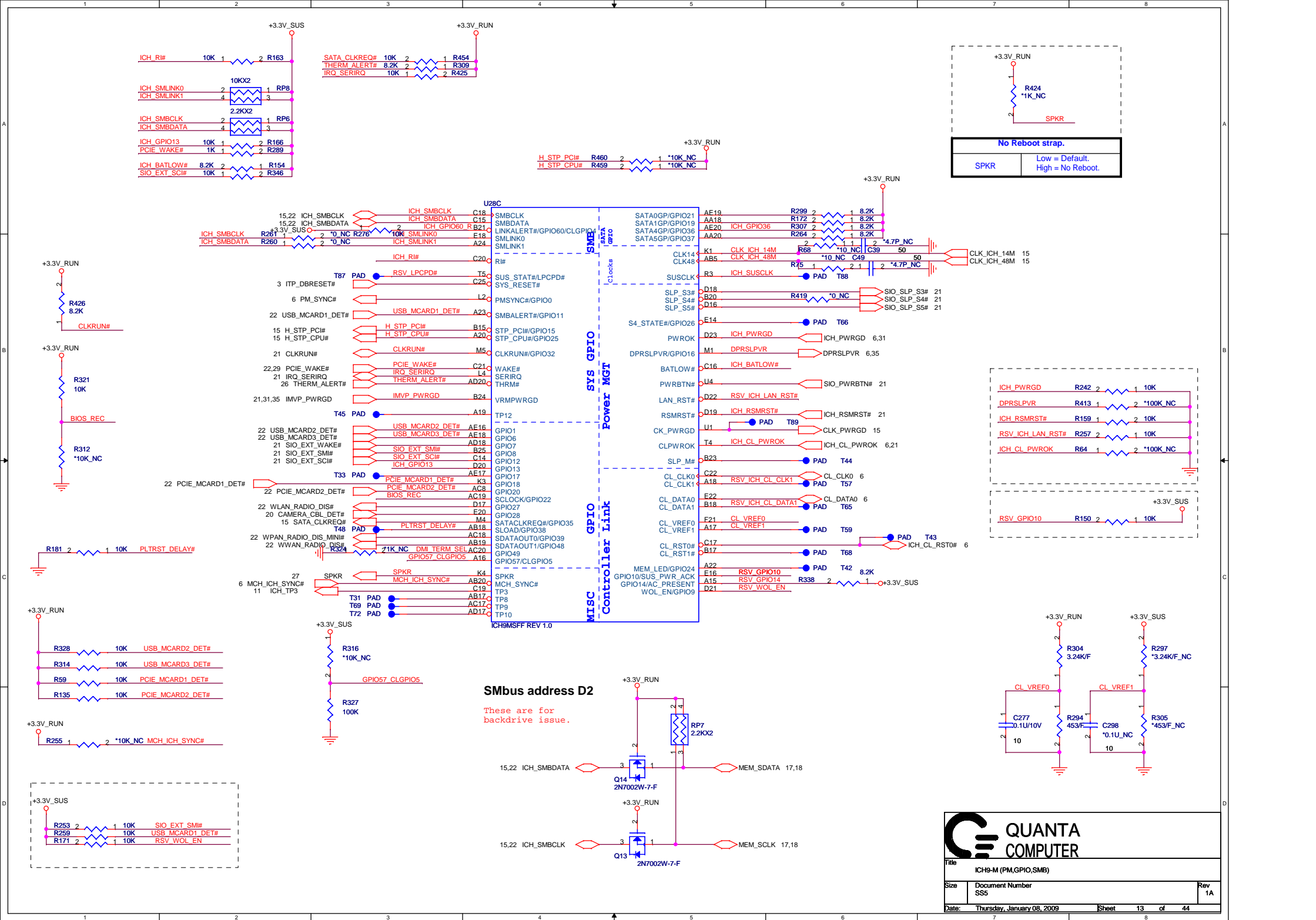
ICH9MSFF REV 1.0

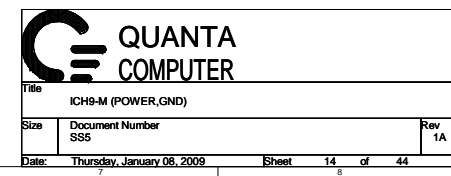
Add Buffers as needed for Loading and fanout concerns.

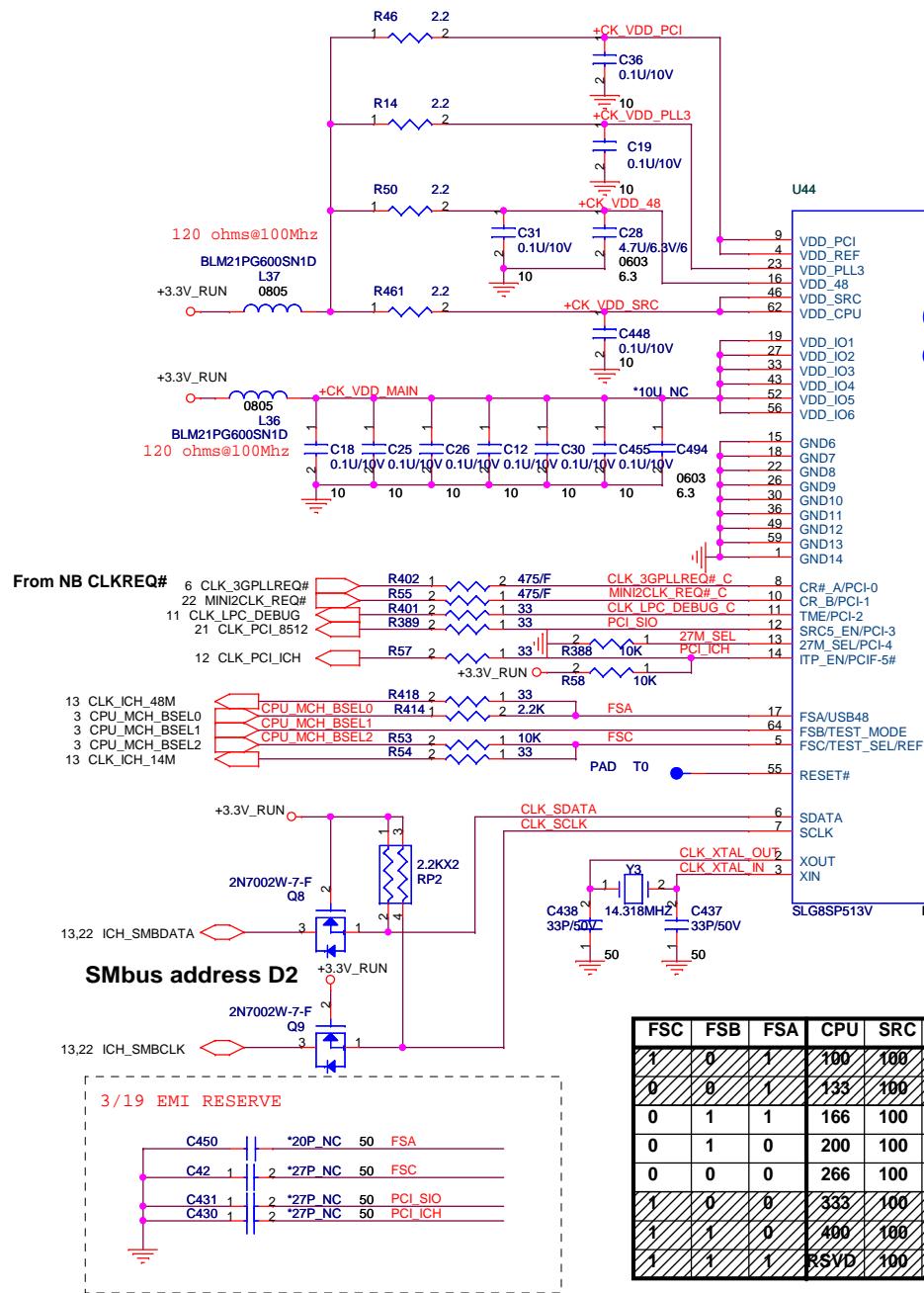
Reserved for EMI.Place resistor and cap close to ICH.



Title ICH9-M(USB,PCIe,DMI)		
Size	Document Number SS5	Rev 1A
Date:	Friday, February 20, 2009	Sheet 12 of 44

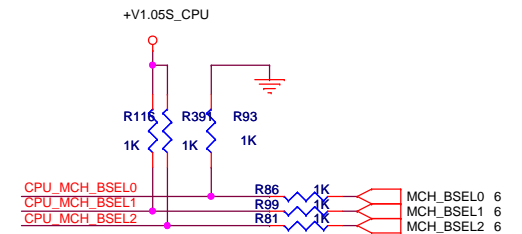
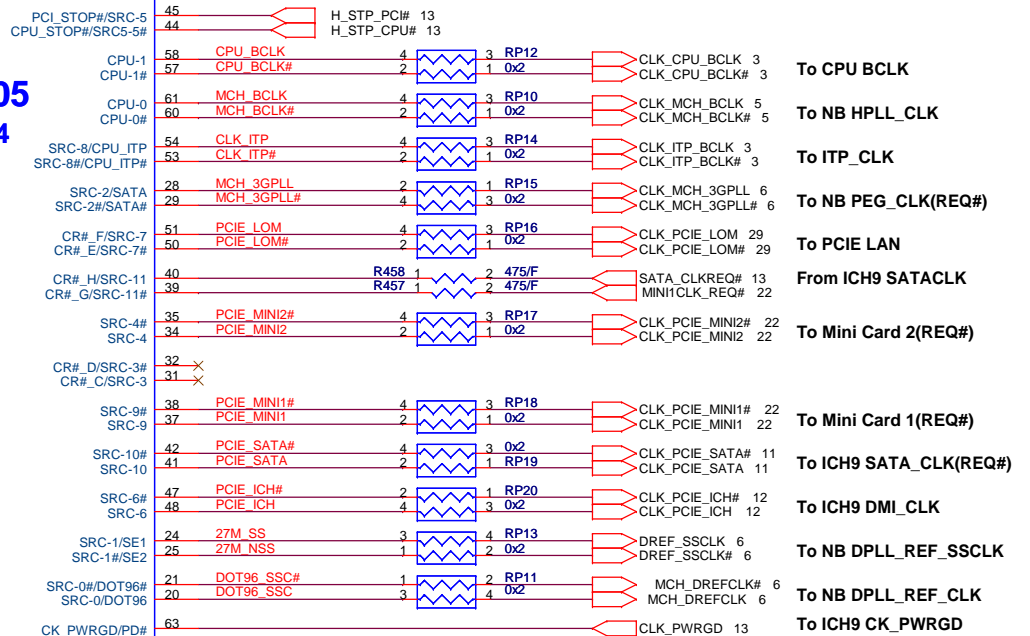
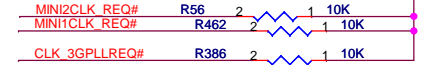




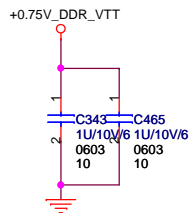


CK505 QFN64

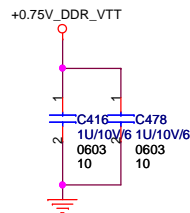
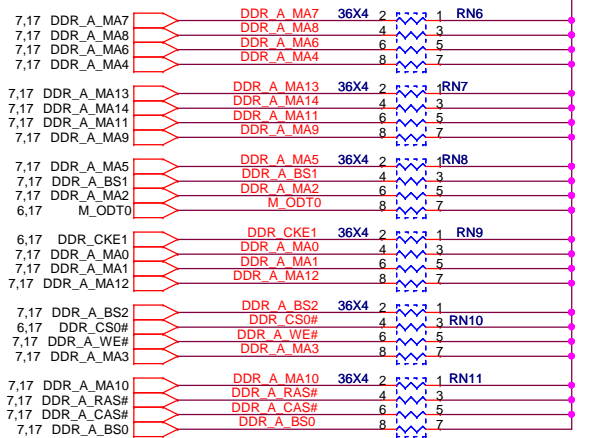
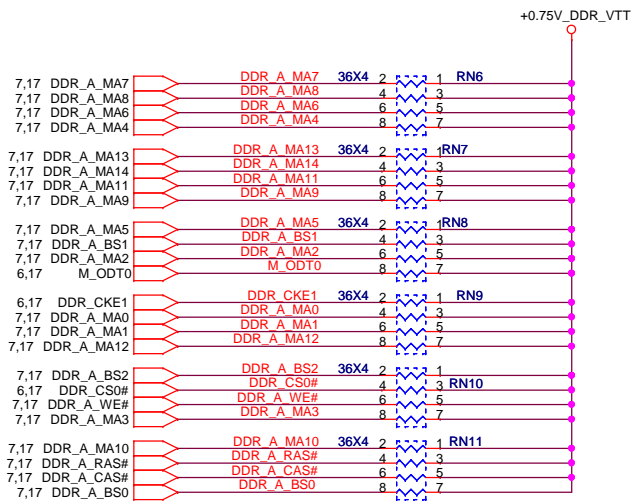
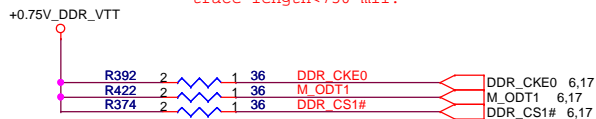
- REQUEST 1. EXPRESS CARD
2. SATA
3. NB
4. BT & UWB



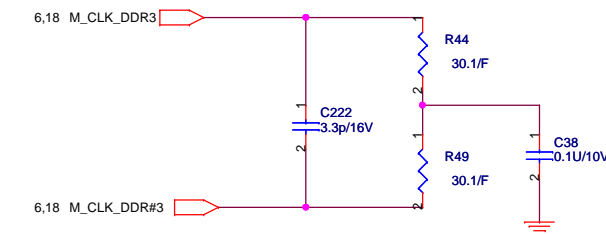
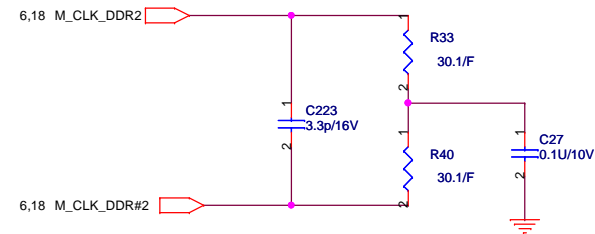
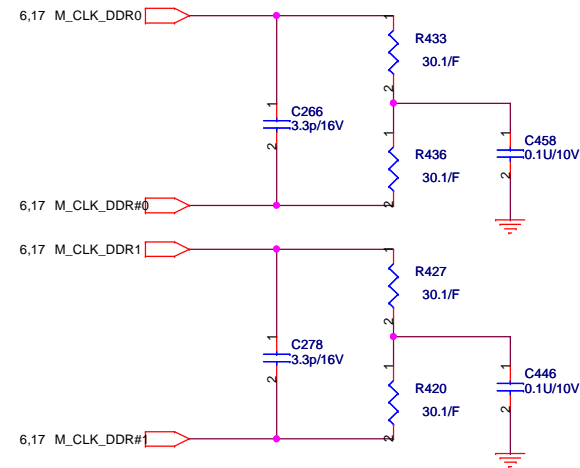
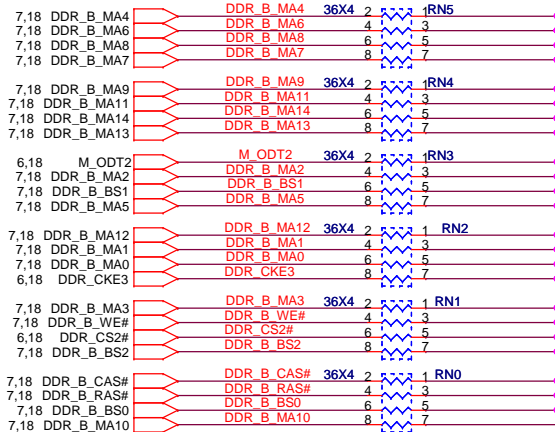
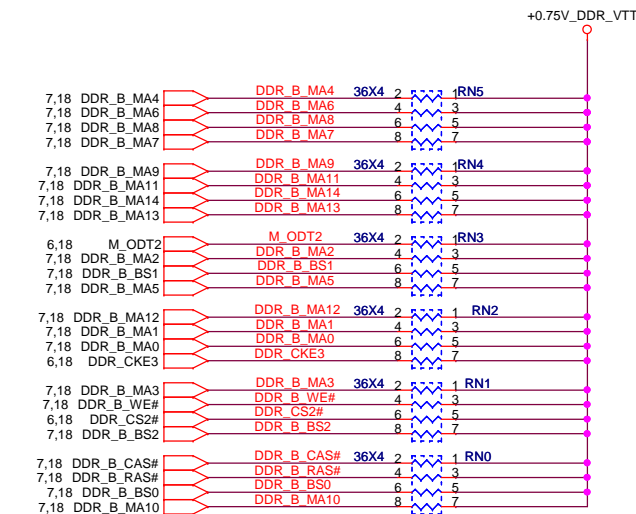
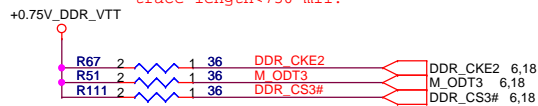
Title CLOCK



Please these resistor
closely DIMMA,all
trace length<750 mil.



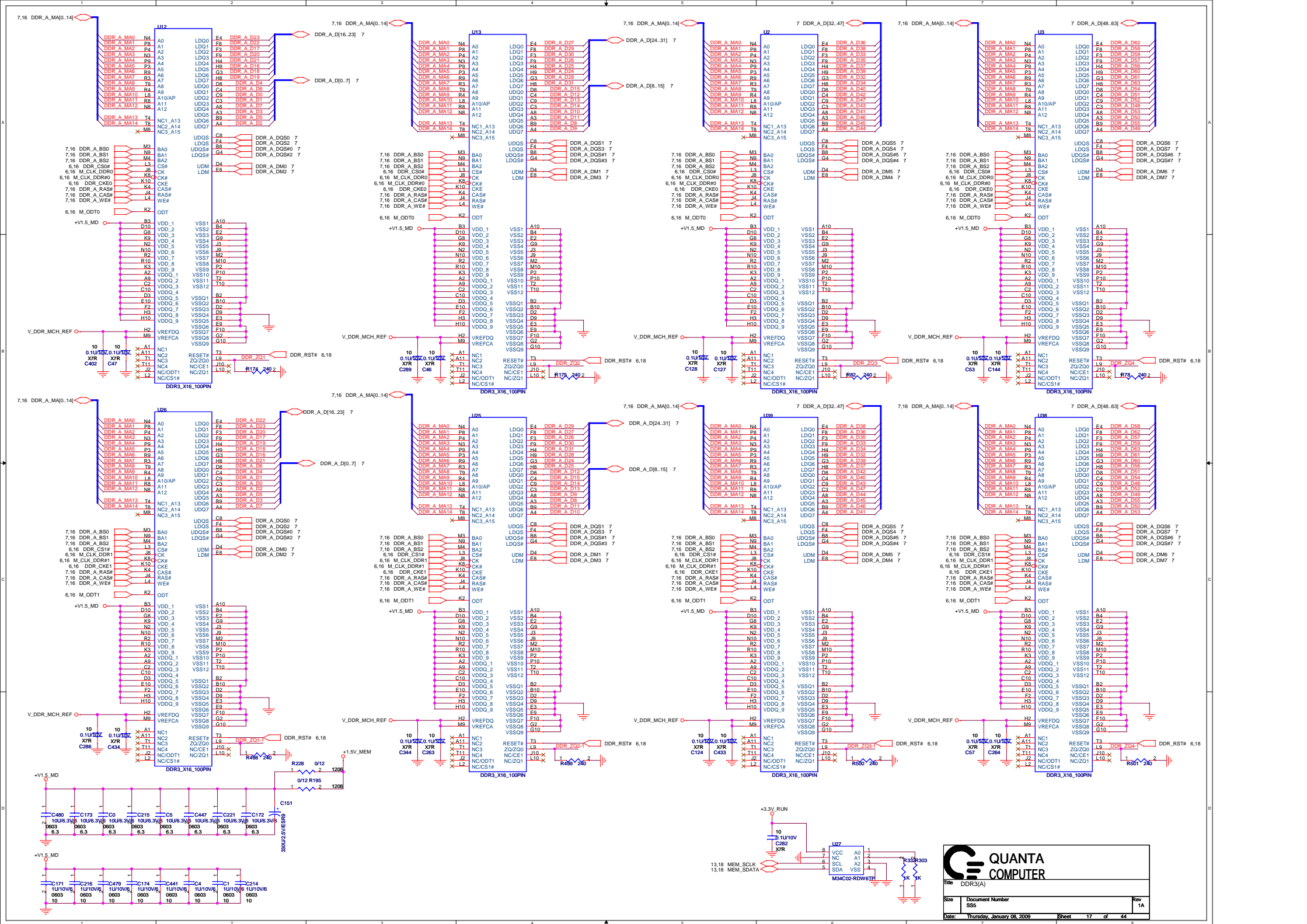
Please these resistor
closely DIMMB,all
trace length<750 mil.

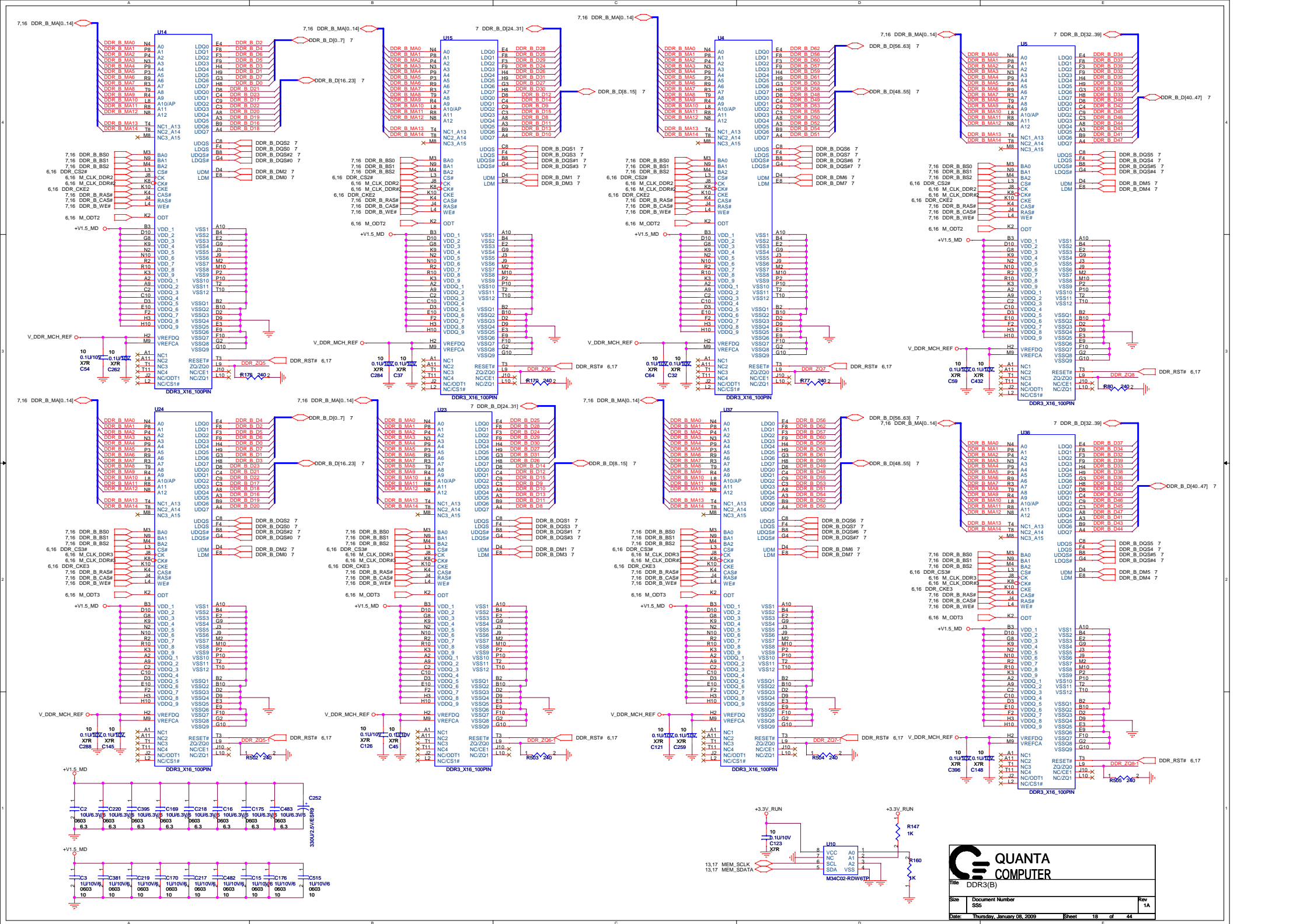


Title DDR3 TERMINATION

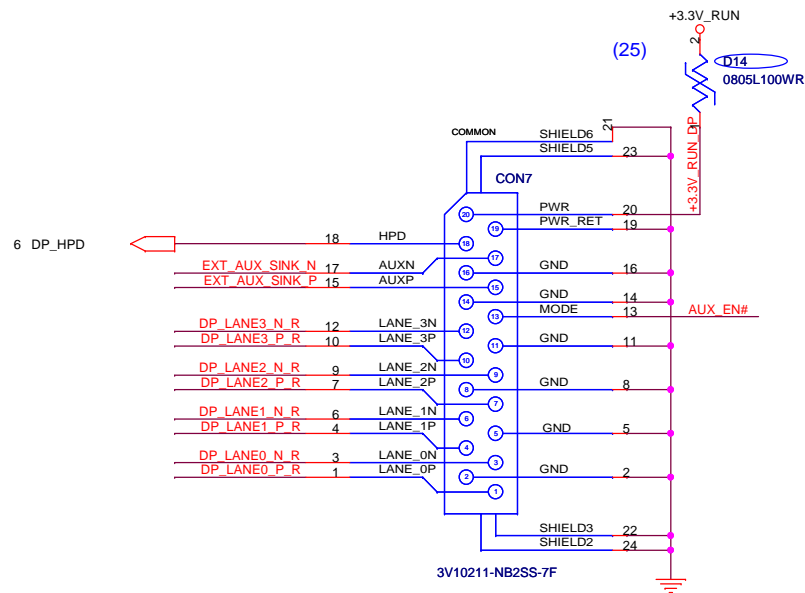
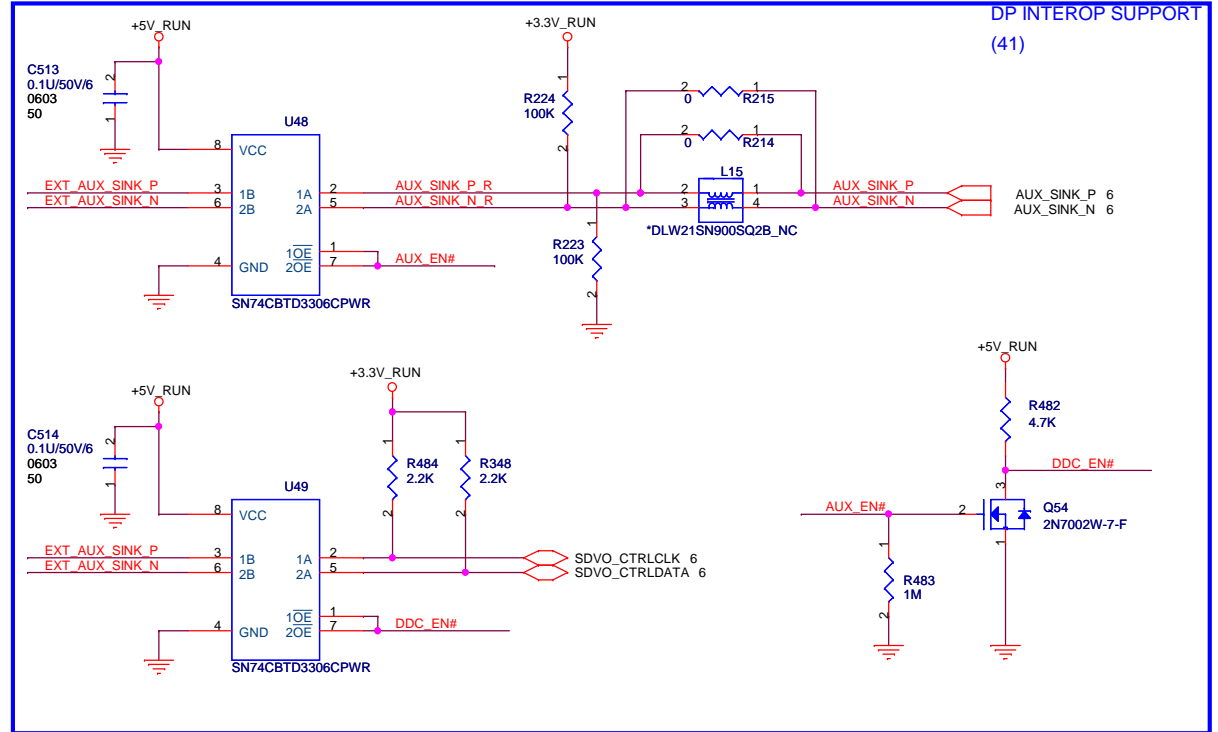
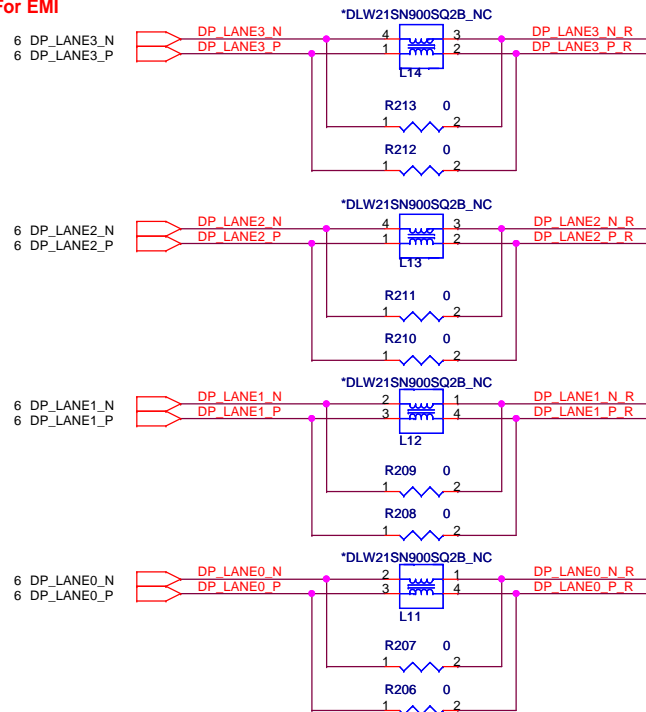
Size	Document Number	Rev
SS5		1A

Date: Thursday, January 08, 2009 Sheet 16 of 44

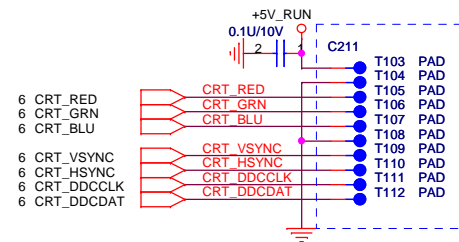




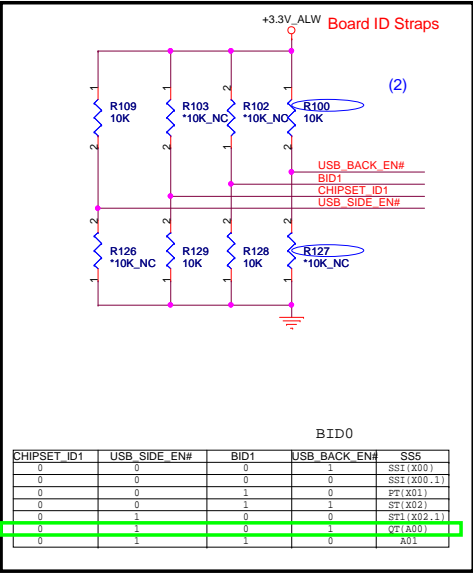
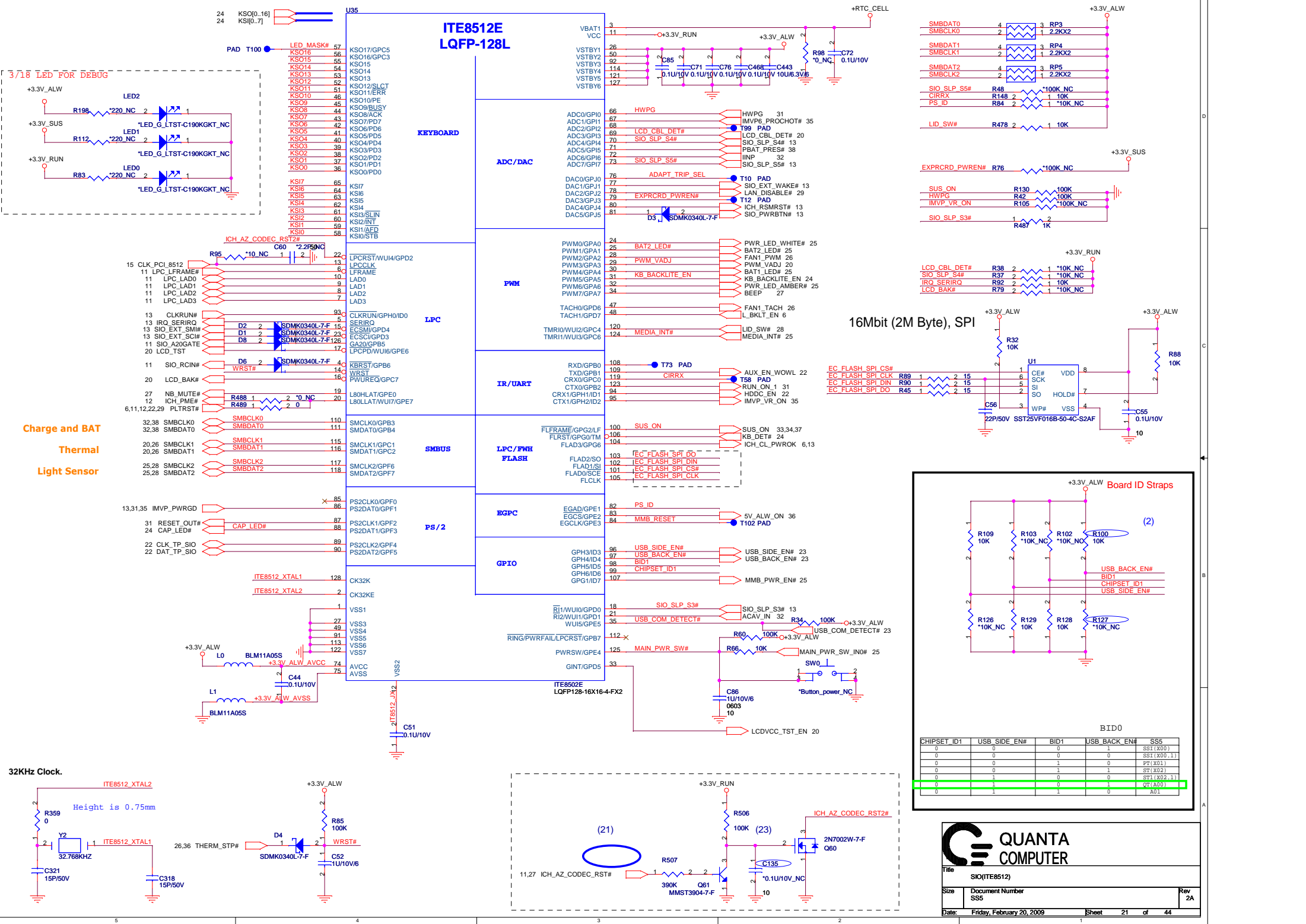
Reserve For EMI




CRT OUT For debug



Title			Display port/CRT Conn
Size	Document Number	Rev	
	SS5	1A	
Date:	Friday, February 20, 2009	Sheet	19 of 44





QUANTA
COMPUTER

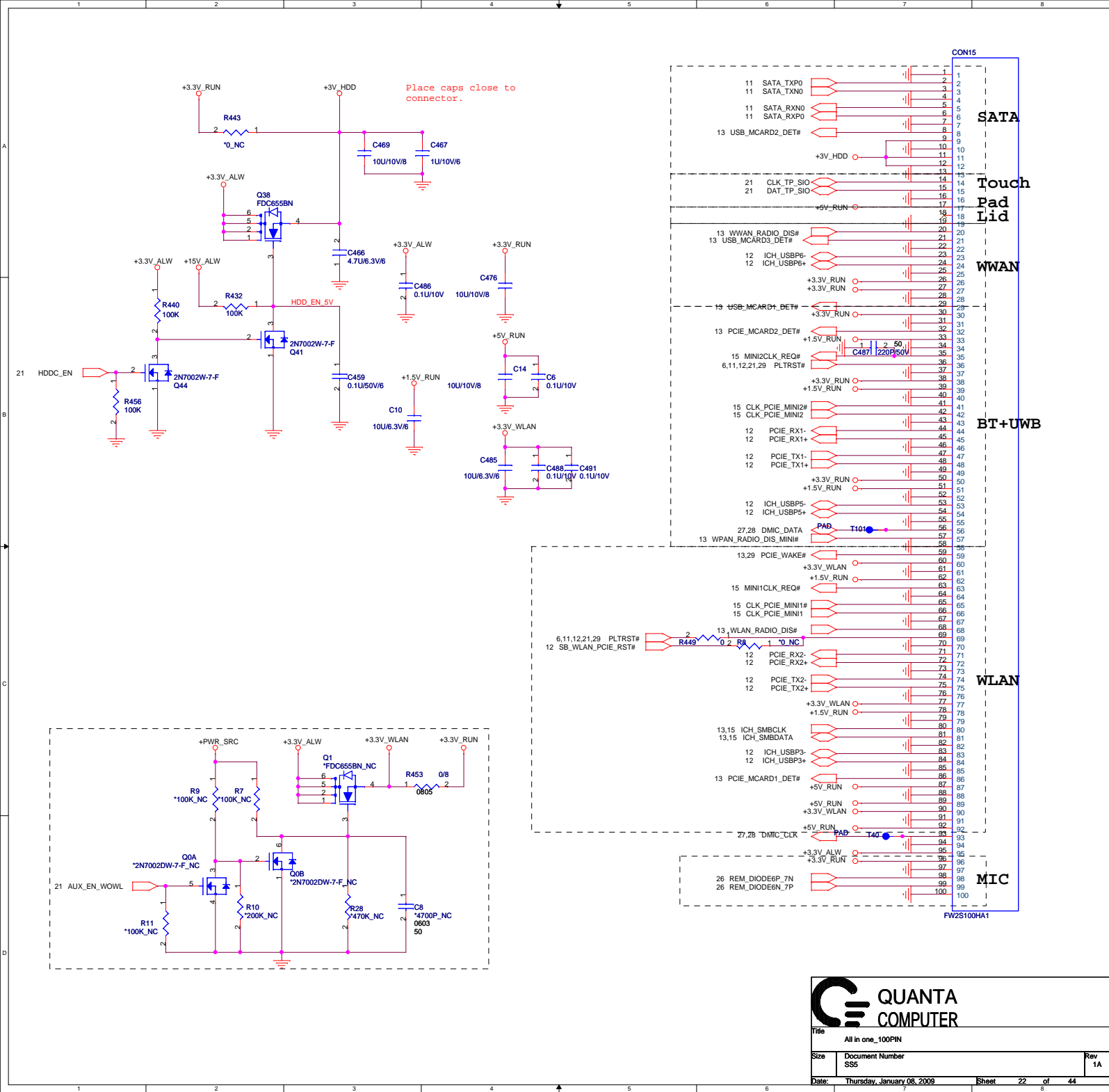
TitleSIO(ITE8512)

SizeDocument NumberSS5

Date:Friday, February 20, 2009

Sheet21 of 44

Rev2A



QUANTA
COMPUTER

Title
All in one_100PIN

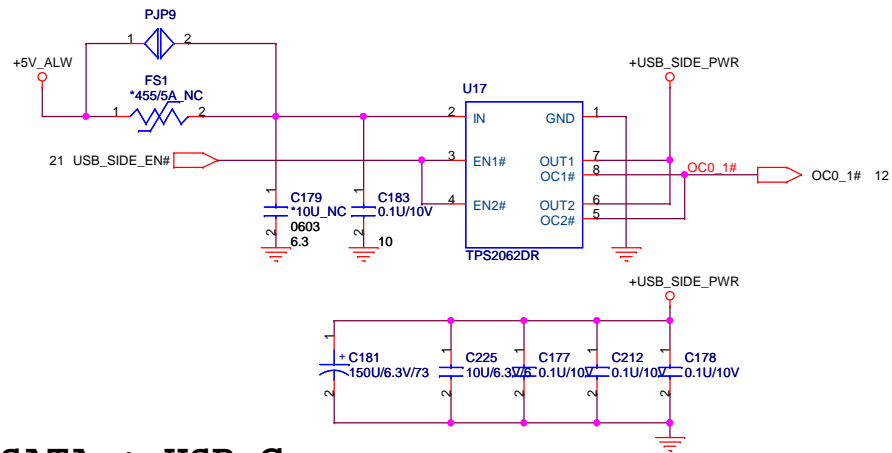
Size
SSS

Date:
Thursday, January 08, 2009

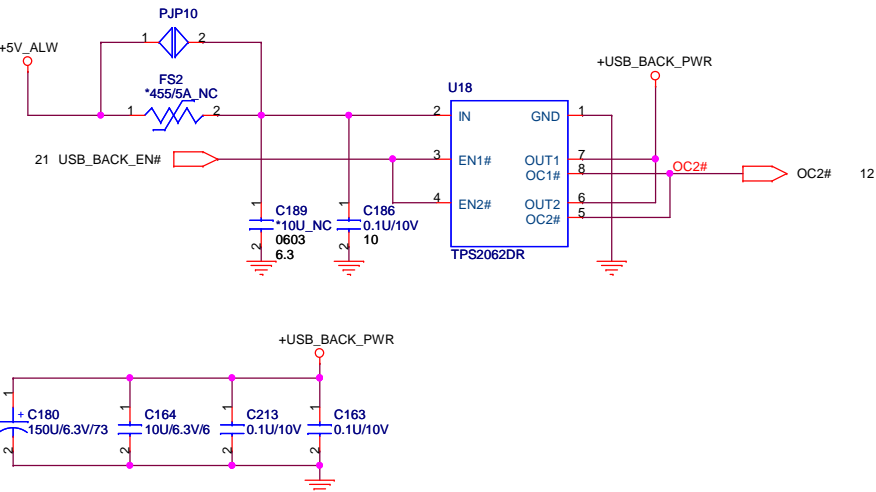
Sheet
22 of 44

Rev
1A

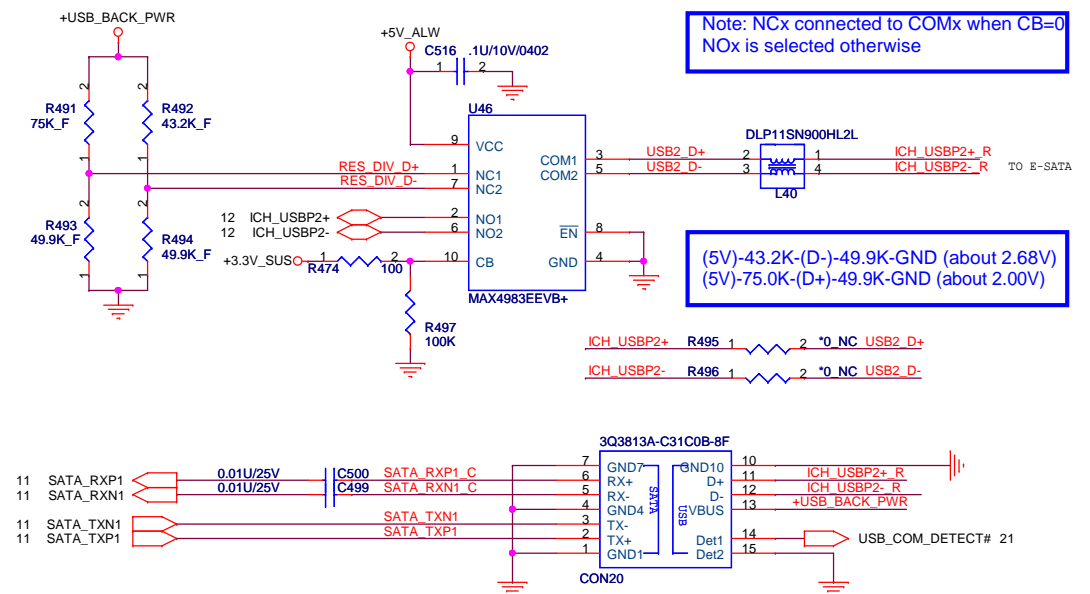
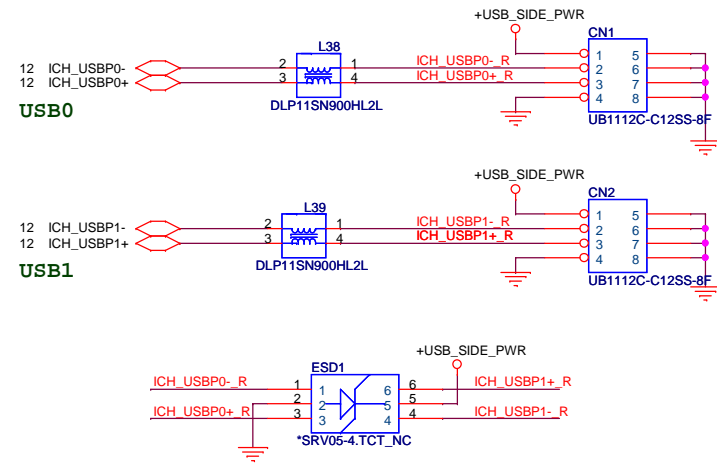
USB x2 Conn



SATA + USB Conn



BATTERY STATUS LED 1



Title	SERIAL PORT & USB
-------	-------------------

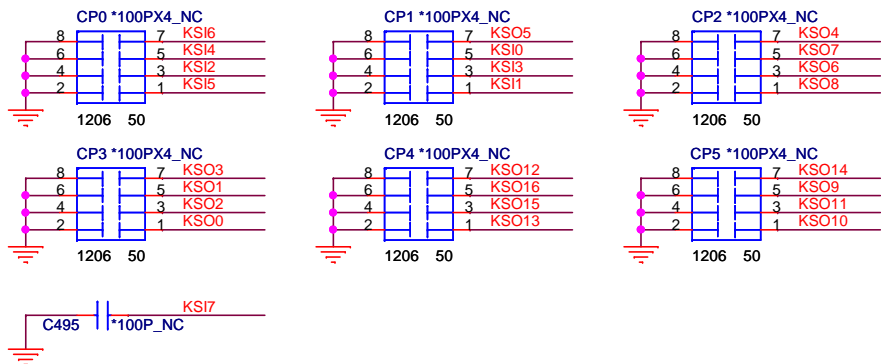
Size	Document Number SS5
------	------------------------

Date: Thursday, February 05, 2009

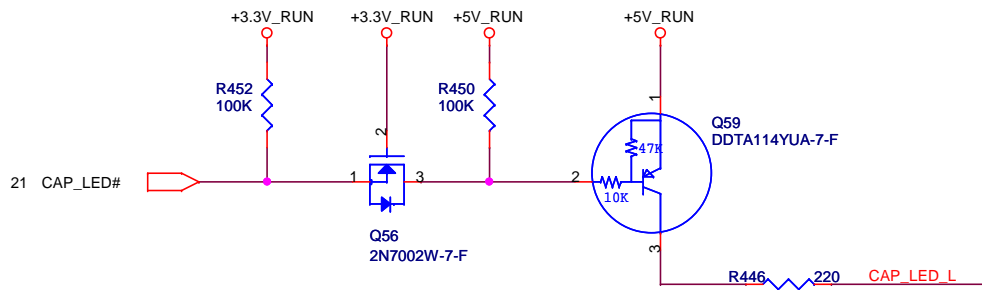
Sheet 23 of 44

ev
1A

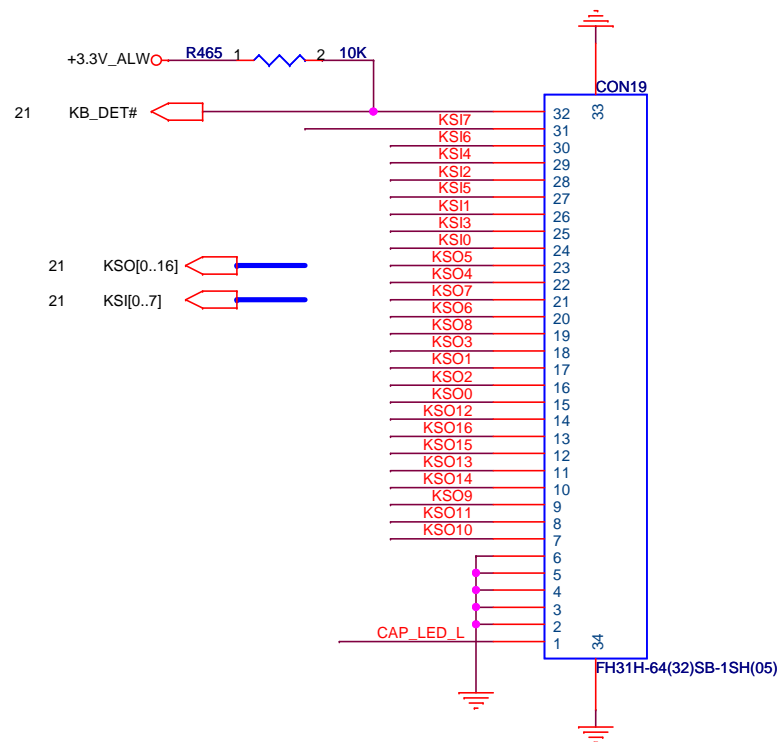
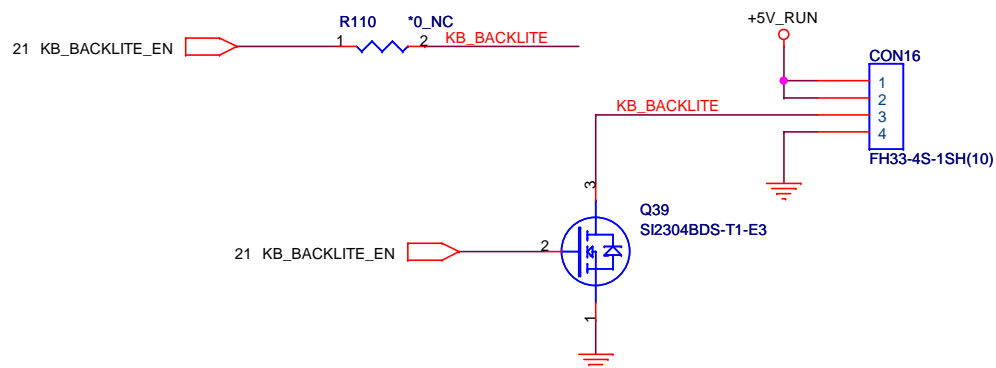
KEYBOARD CONNECTOR



CAP_LED#

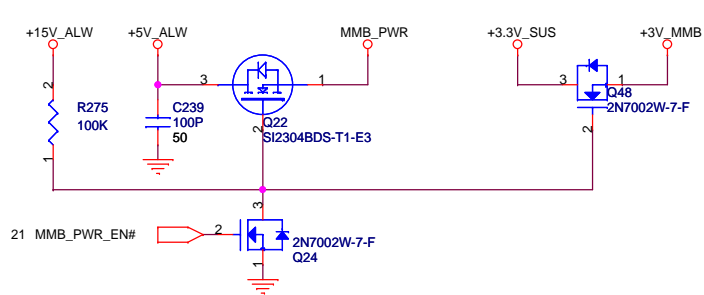


KB LED CONN



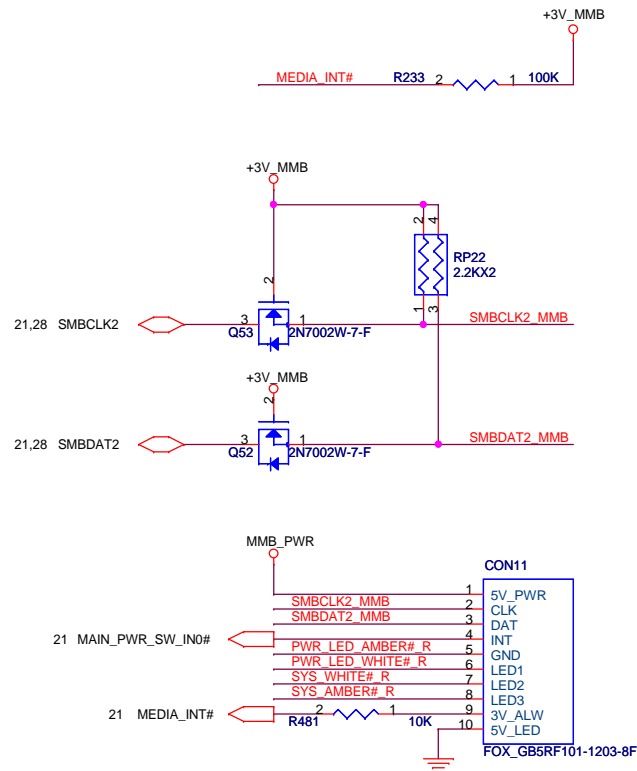
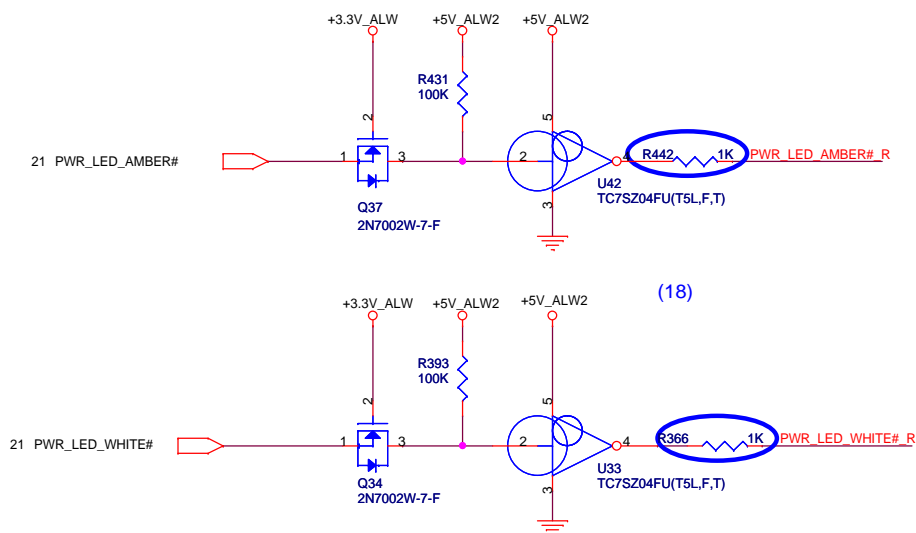
100P CAPS CLOSE TO JKB1

QUANTA COMPUTER	
Title TOUCH PAD, BULE TOOTH & FIR	
Size SS5	Document Number
Date: Thursday, January 08, 2009	
Sheet 24 of 44	
Rev 2A	

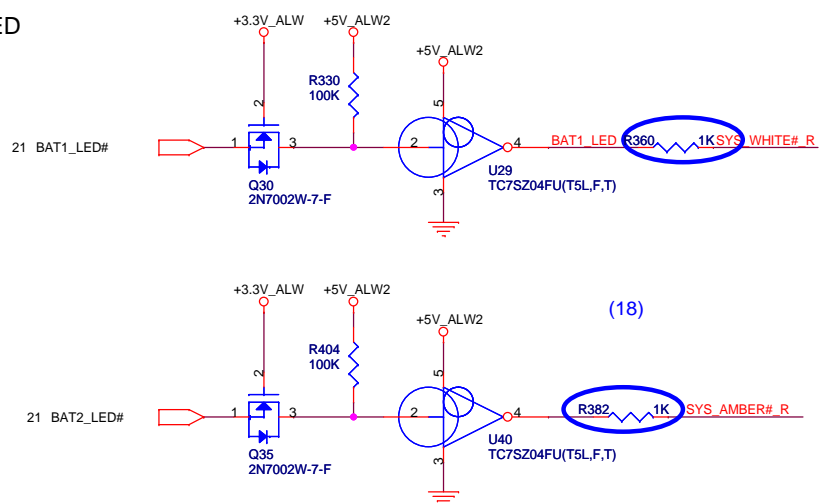


POWER LED

Function board CONN



System LED



System Power State	Power Source	Battery Charge State	LED Behavior
On (S0)	AC	0-100%	Off
On (S0)	DC	< 10%	Flash Amber
On (S0)	DC	> 10%	Off
Standby (S3)	AC	0-100%	"Breathe" White
Standby (S3)	DC	< 10%	Flash Amber
Standby (S3)	DC	> 10%	"Breathe" White
Off or Hibernate (S4/S5)	AC	< 90%	Solid Amber
Off or Hibernate (S4/S5)	AC	> 90%	Solid White
Off or Hibernate (S4/S5)	DC	0-100%	Off



QUANTA
COMPUTER

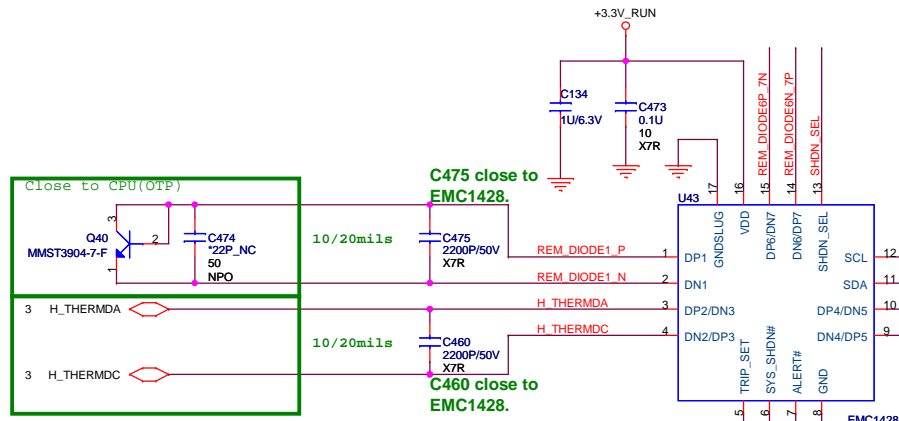
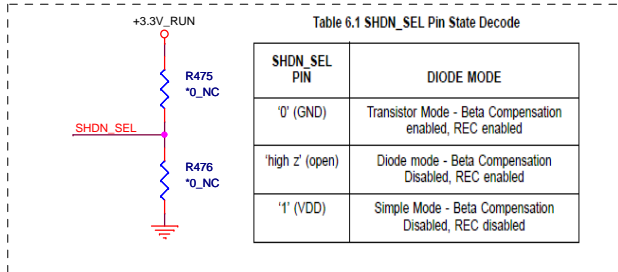
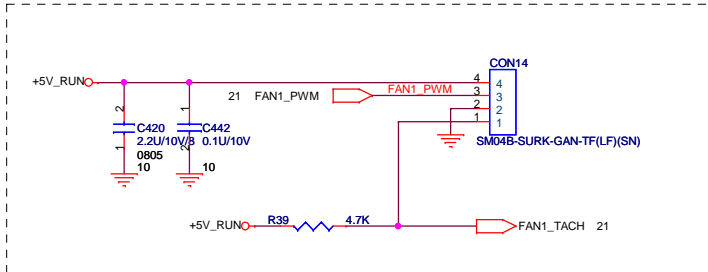
Title
SWITCH, KEYBOARD & LED

Size
Document Number
SS5

Rev
1A

Date: Thursday, February 05, 2009

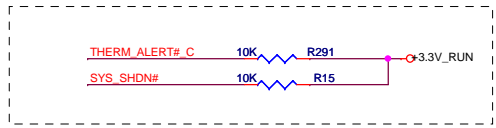
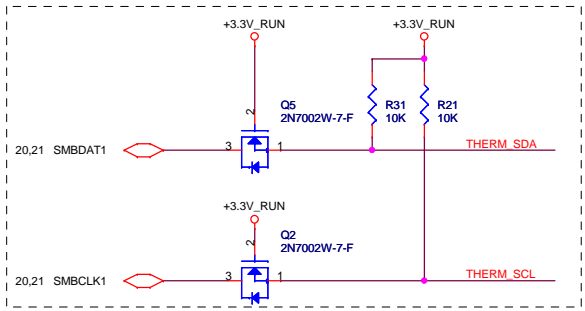
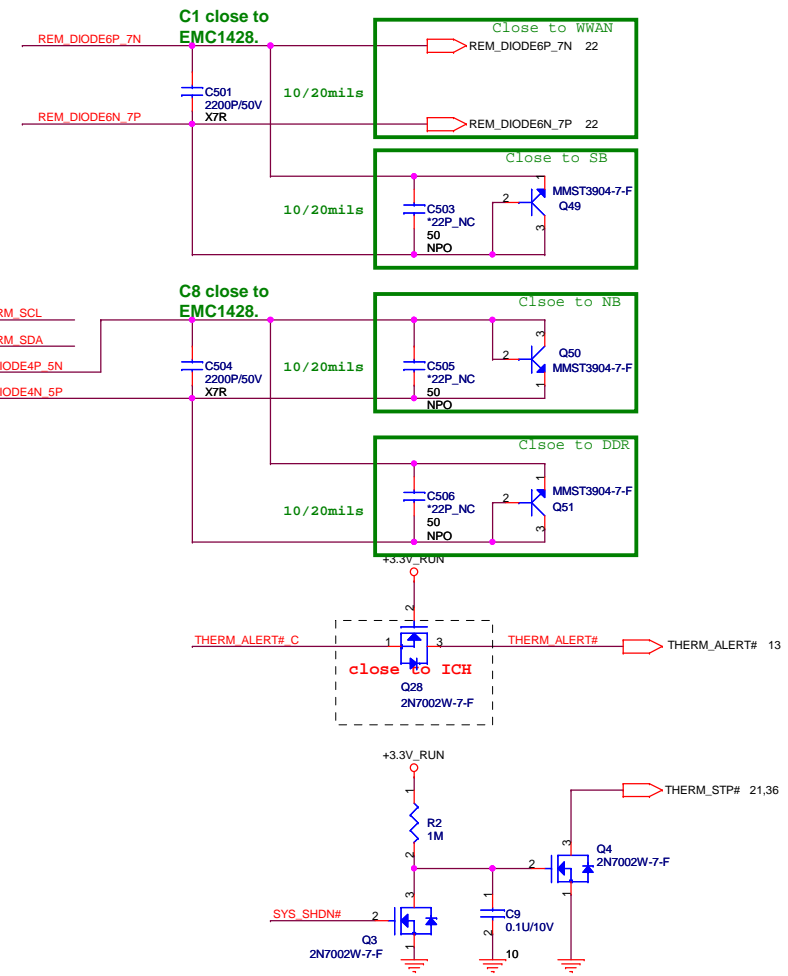
Sheet 25 of 44



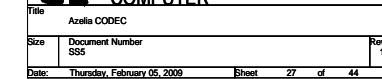
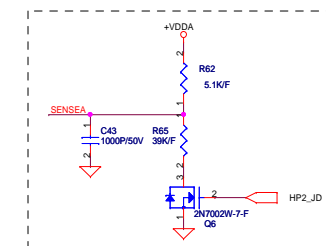
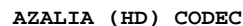
OTP 83 degree C

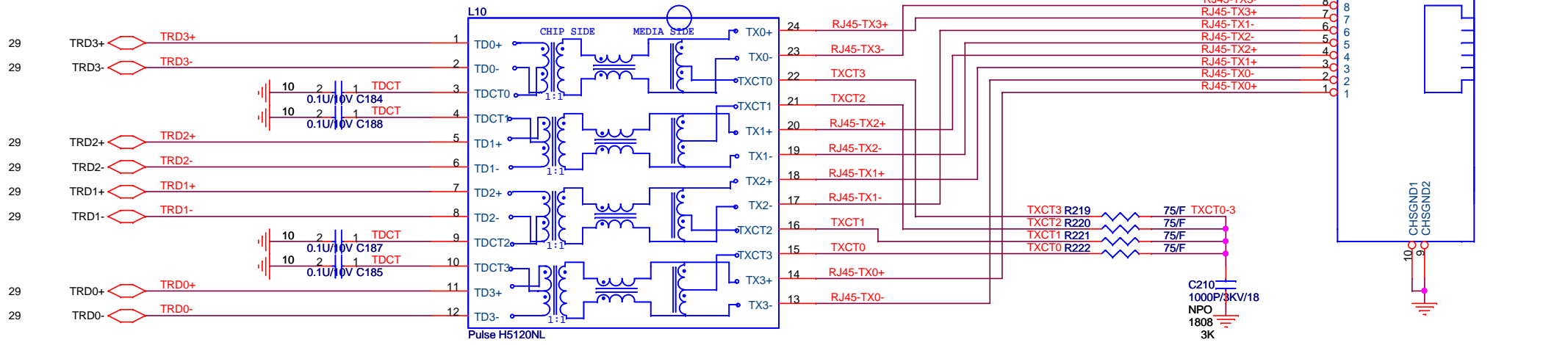
Example set points:
TTrip_RSet

Degree C	R477
65	0
75	237
83	487
85	562
95	1100
121	9090



INTERNAL SPEAKER AMP






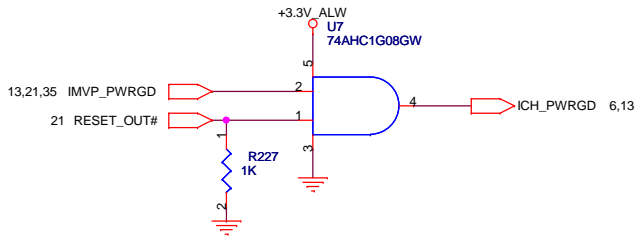
Reserved for EMI.

TRD3+	C191	6.8P/50V
TRD3-	C190	6.8P/50V
TRD2+	C194	6.8P/50V
TRD2-	C195	6.8P/50V
TRD1+	C196	6.8P/50V
TRD1-	C197	6.8P/50V
TRD0+	C192	6.8P/50V
TRD0-	C193	6.8P/50V

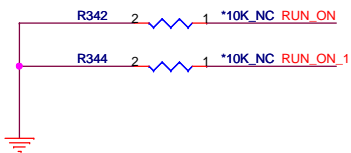
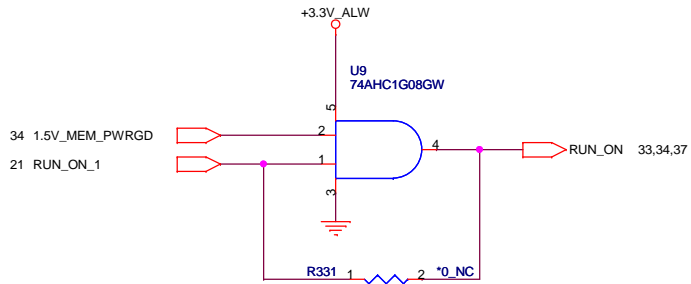
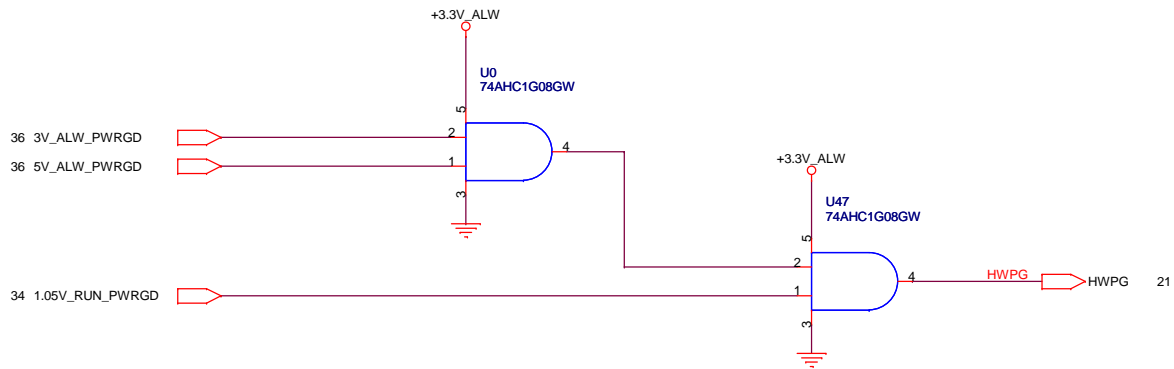
LAYOUT NOTE:
CAP CLOSE TO TRANSFORMER
one cap for each pin


**QUANTA
COMPUTER**

Title LAN SWITCH		
Size	Document Number SS5	Rev 1A
Date:	Thursday, January 08, 2009	Sheet 30 of 44



Keep Away from high speed buses

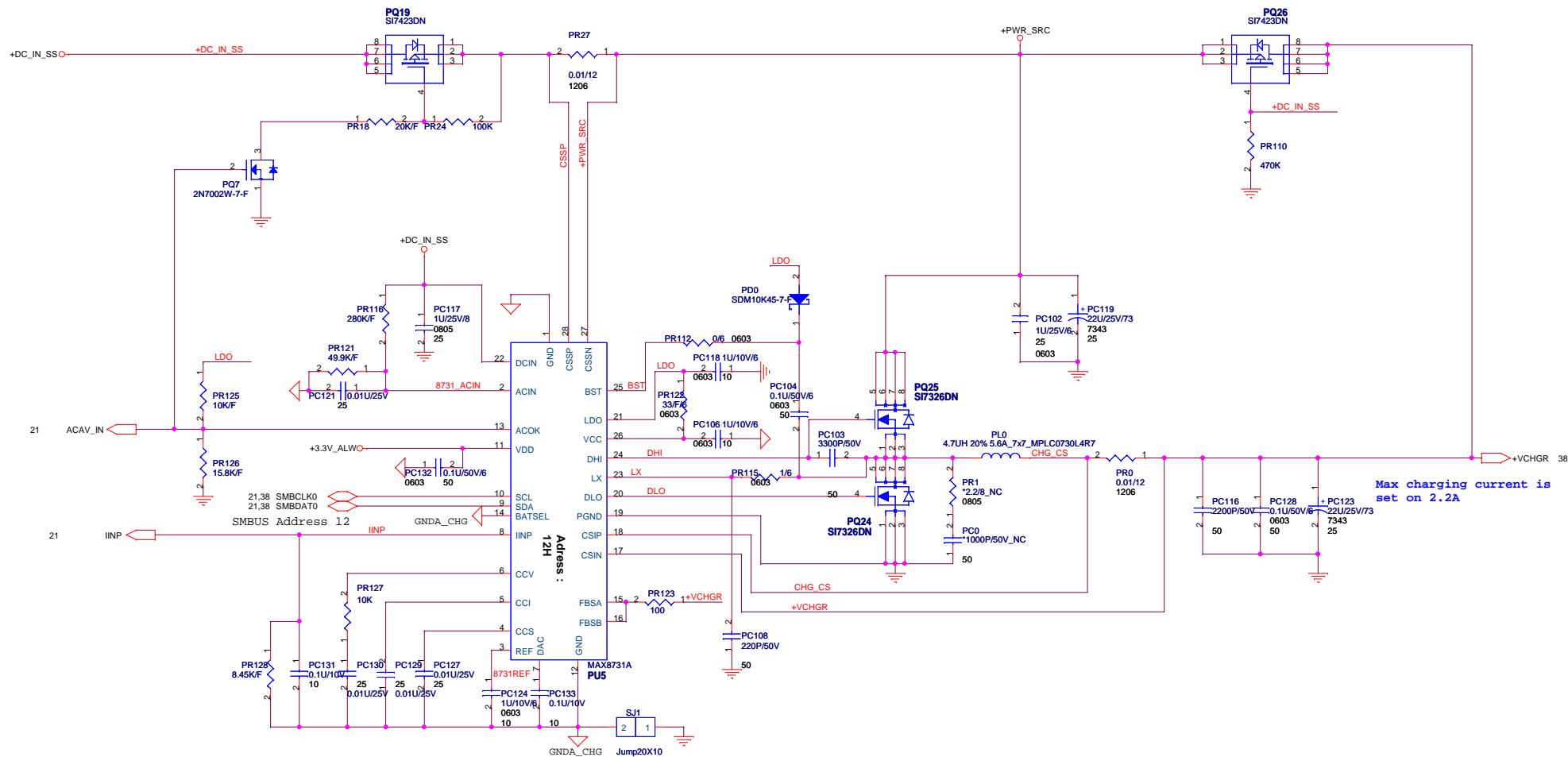




QUANTA

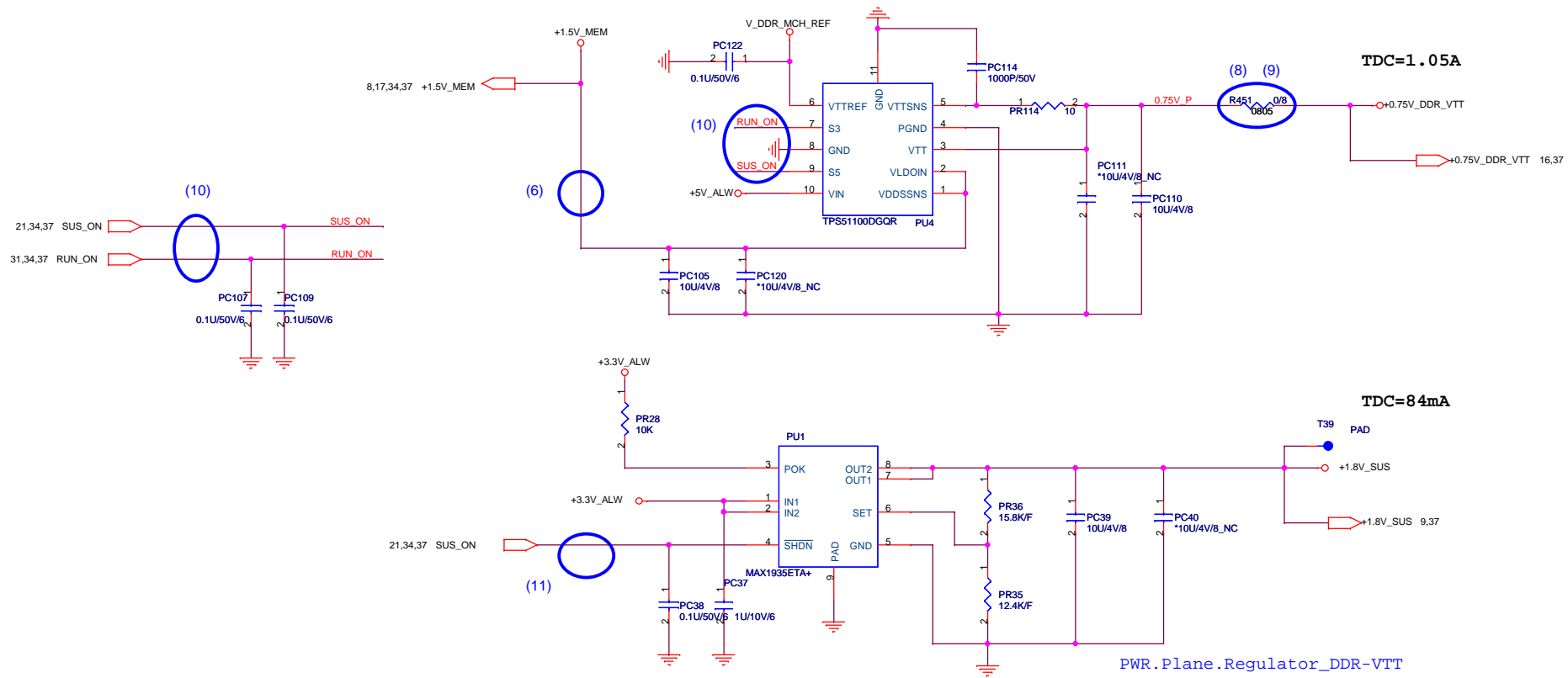
COMPUTER

Title System Reset Circuit		
Size	Document Number SSS	Rev 1A
Date:	Thursday, January 08, 2009	Sheet 31 of 44

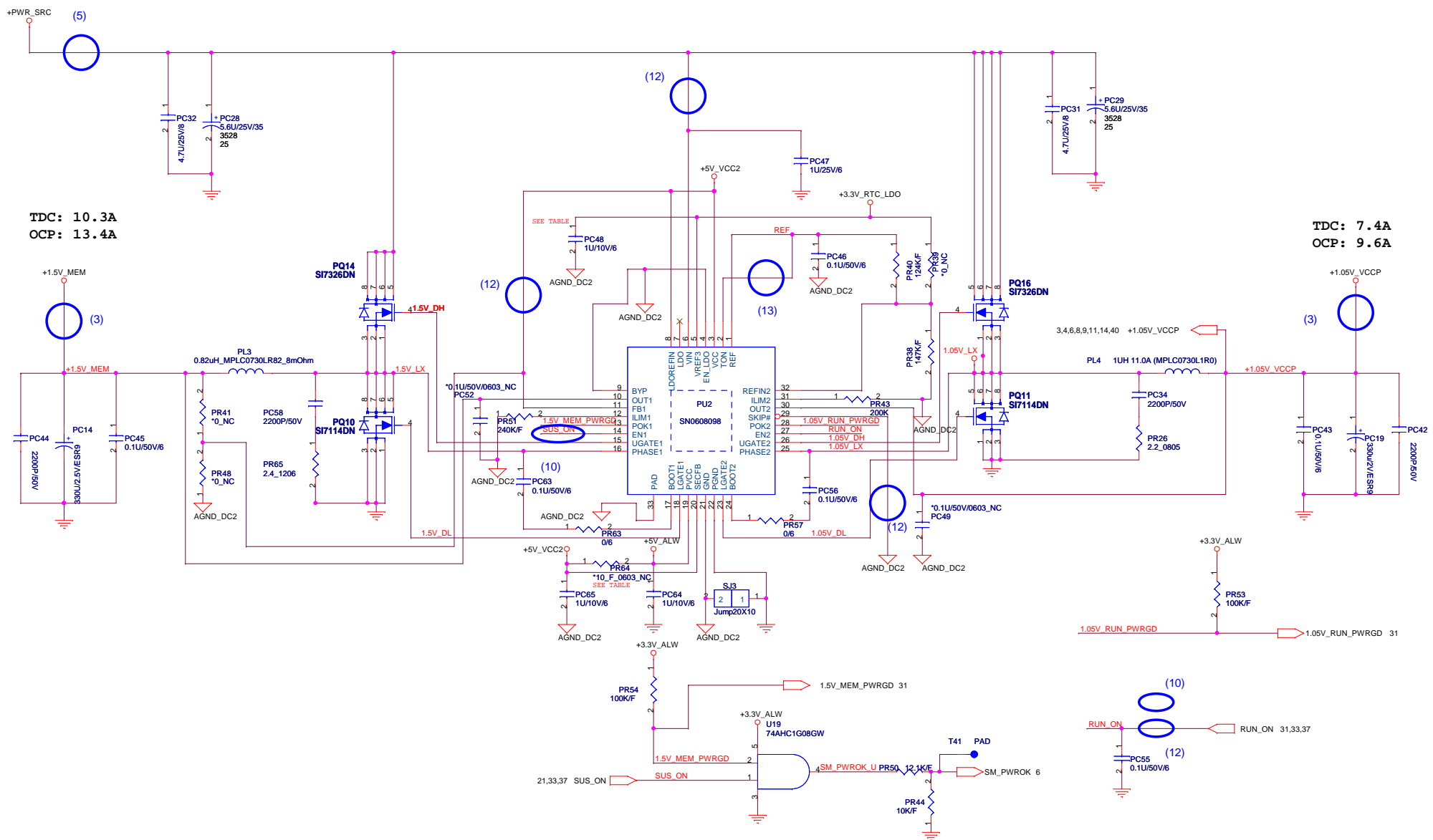


QUANTA
COMPUTER

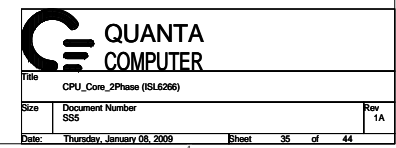
Title			Charger (MAX8731)
Size	Document Number	Rev	
SS5		1A	
Date:	Thursday, January 08, 2009	Sheet	32 of 44



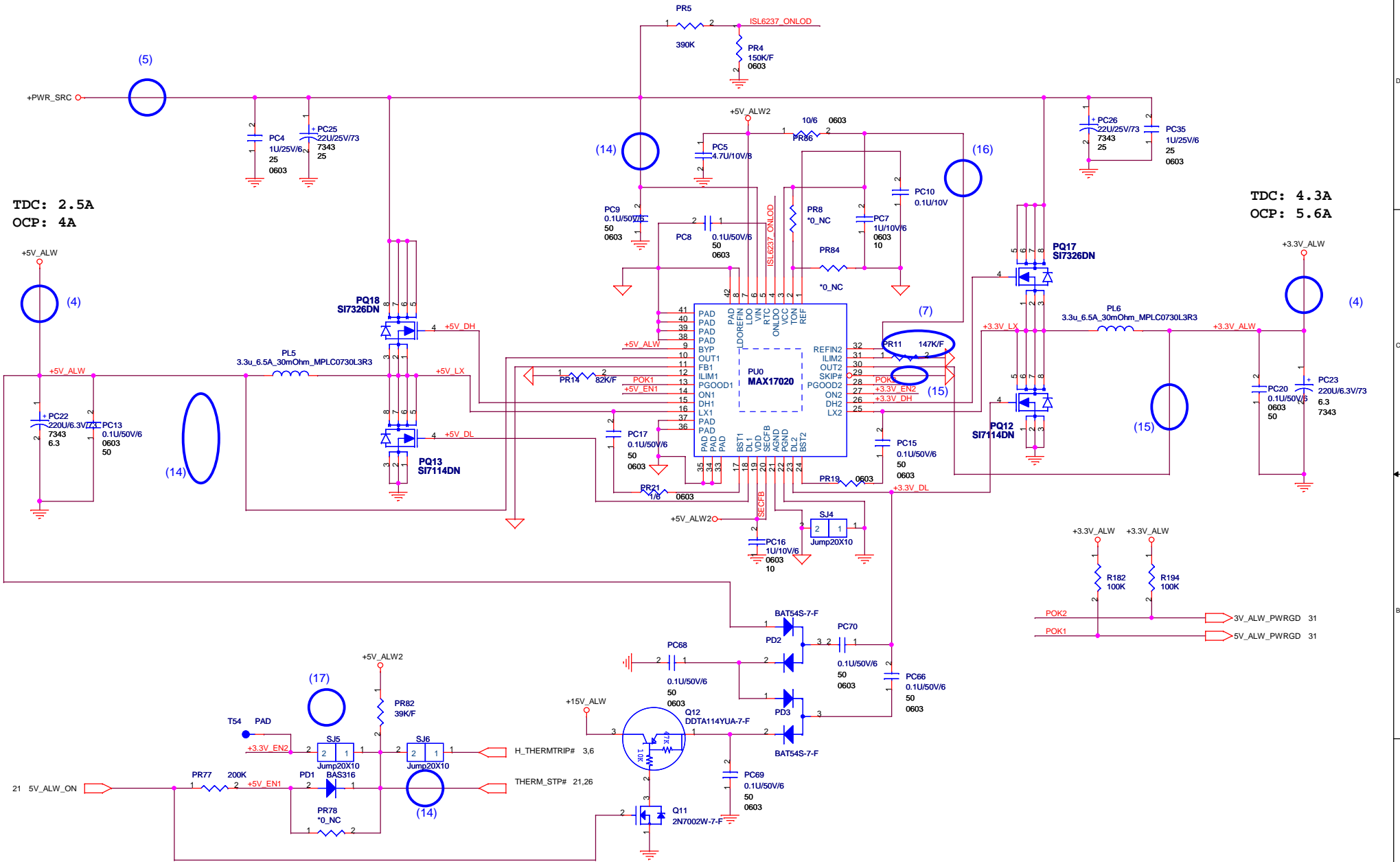
+1.5V_MEM /+1.05V_VCCP /+3.3_RTC_LDO

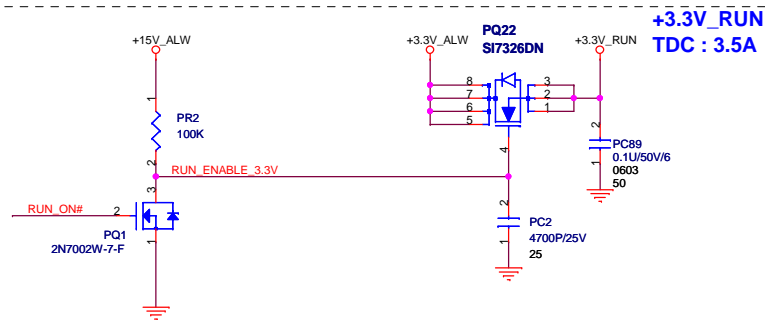
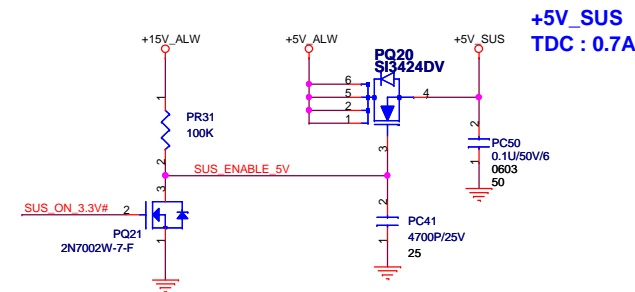
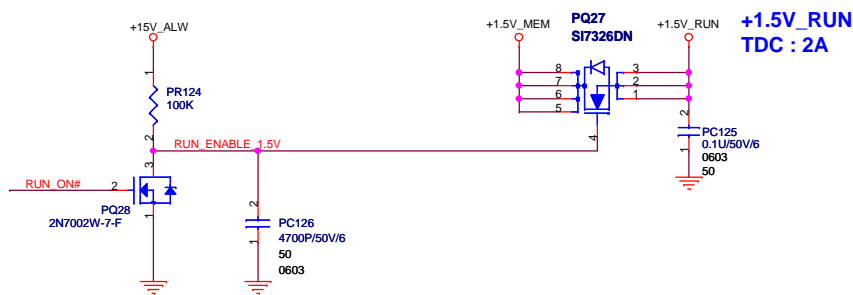
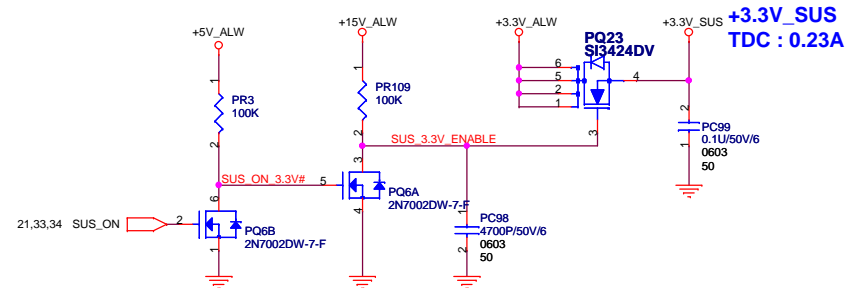
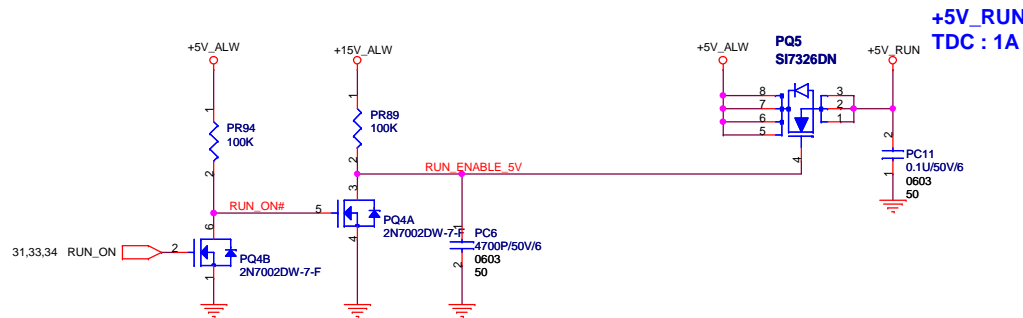


REF DESIGNATOR	MAXIM	INTERSIL	TI
PR64	10, 0603	NO STUFF	NO STUFF
PC48	1uF	0.1uF	1uF

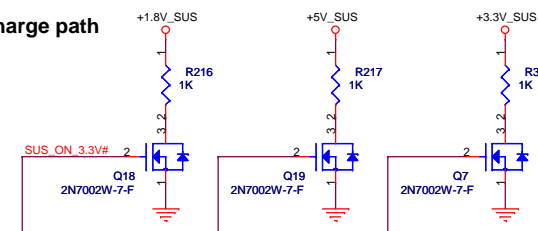


DC/DC +3V_ALW/+5V_SUS/+5V_ALW /+15V_ALW

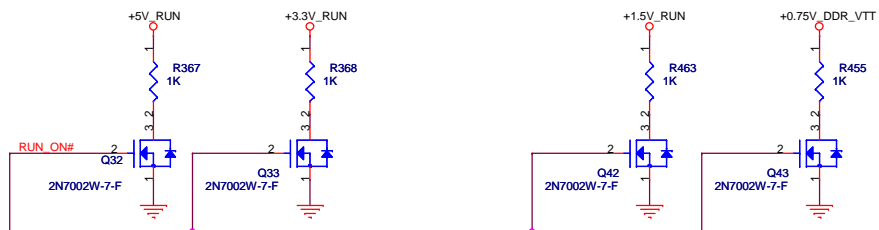




Reserve discharge path

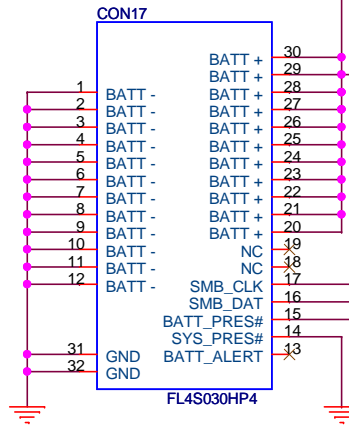
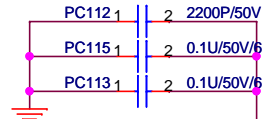


Reserve discharge path



Title			RUN POWER SW
Size	Document Number	Rev	
SS5		1A	
Date:	Friday, February 20, 2009	Sheet	37 of 44

Address : 16H

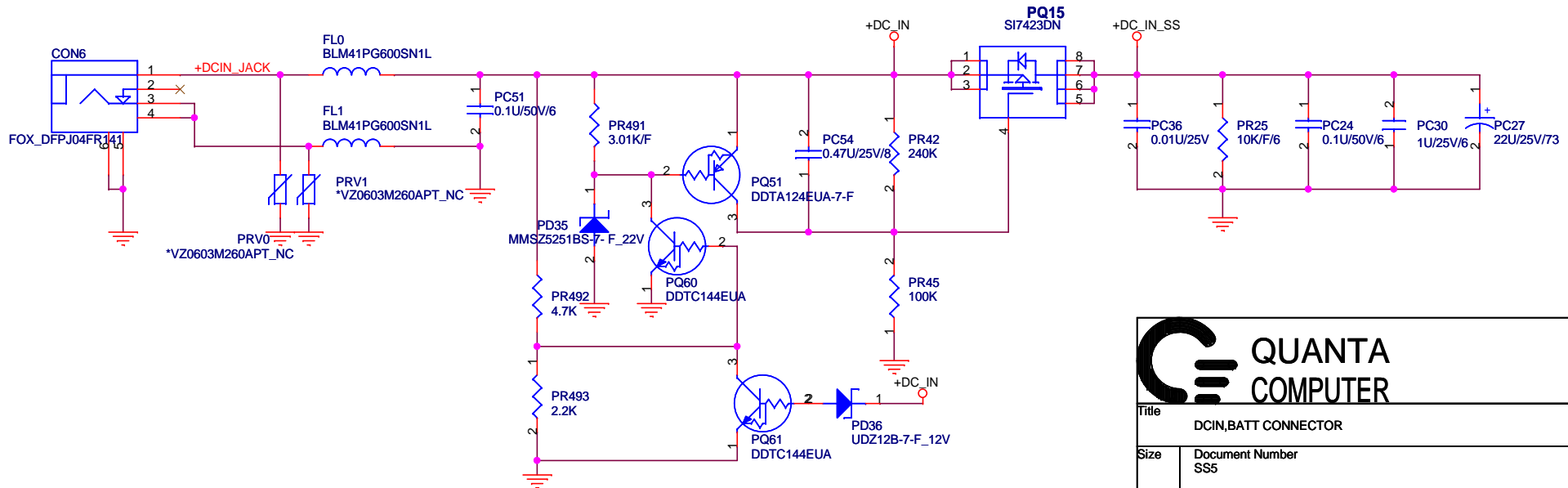


SMBUS Address 16

+3.3V_ALW

PR111
10K

PBAT_PRES# 21



QUANTA COMPUTER

Title: DCIN,BATT CONNECTOR

Size: SS5

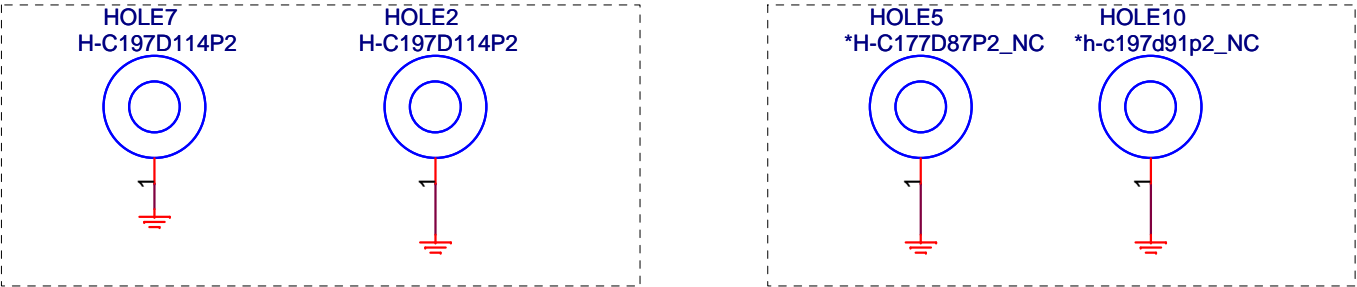
Document Number: SS5

Rev: 1A

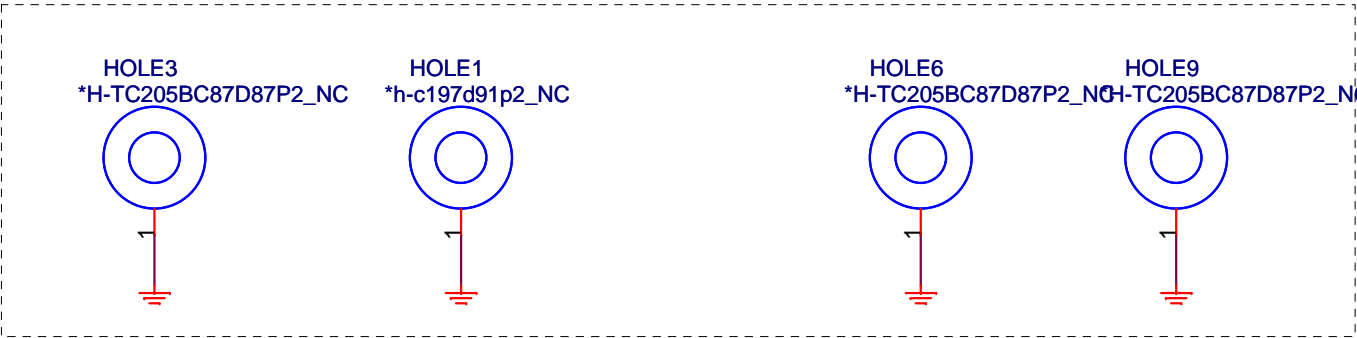
Date: Thursday, February 05, 2009

Sheet: 38 of 44

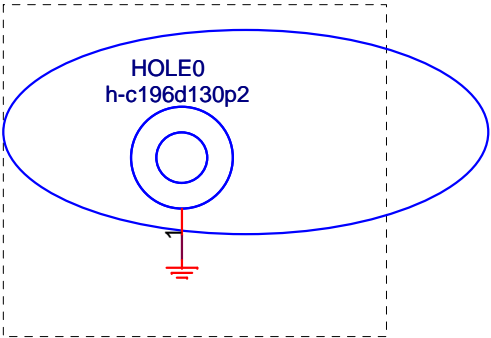
Thermal Screw




Housing Screw



Outer diameter = 4.5mm



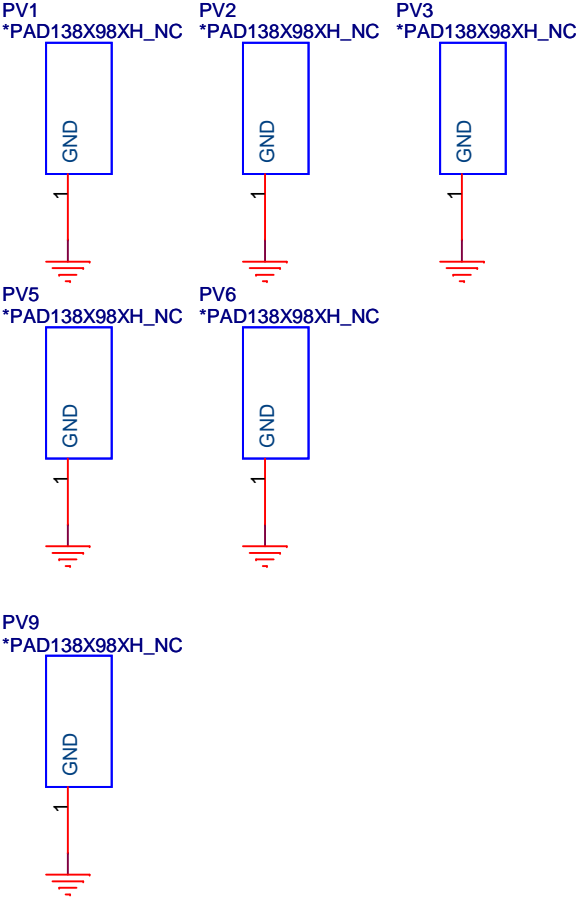
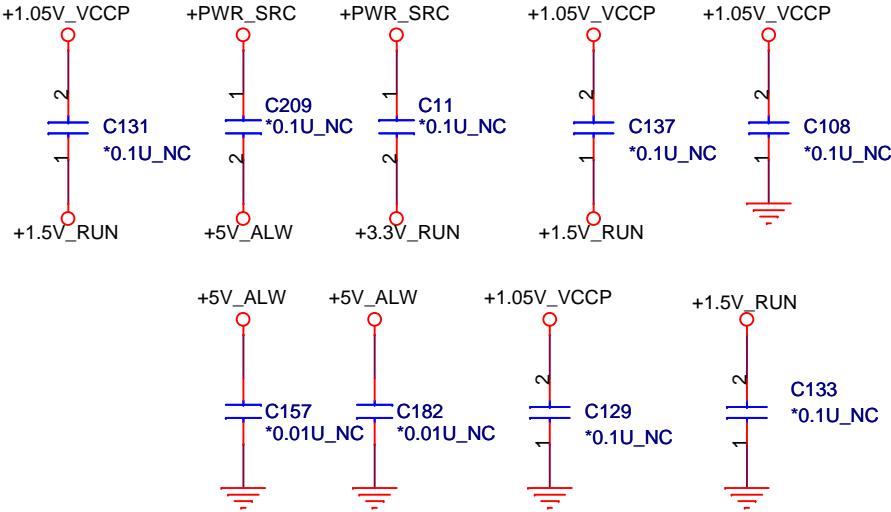
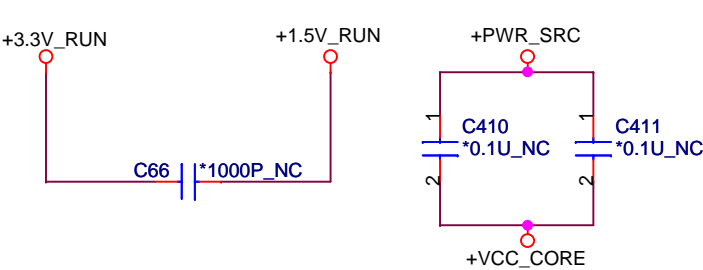
P/N is ok.
Also need change FP 12/29.



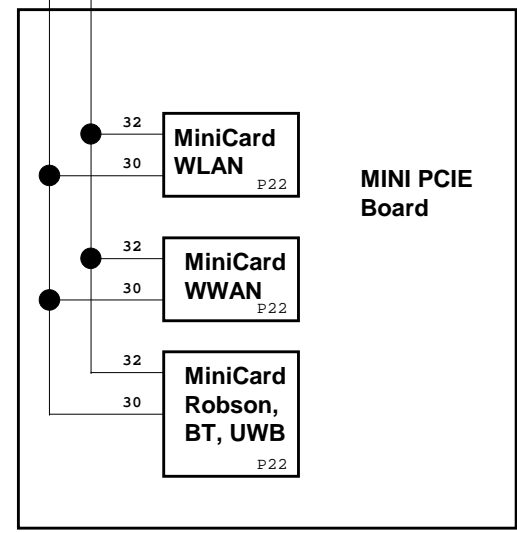
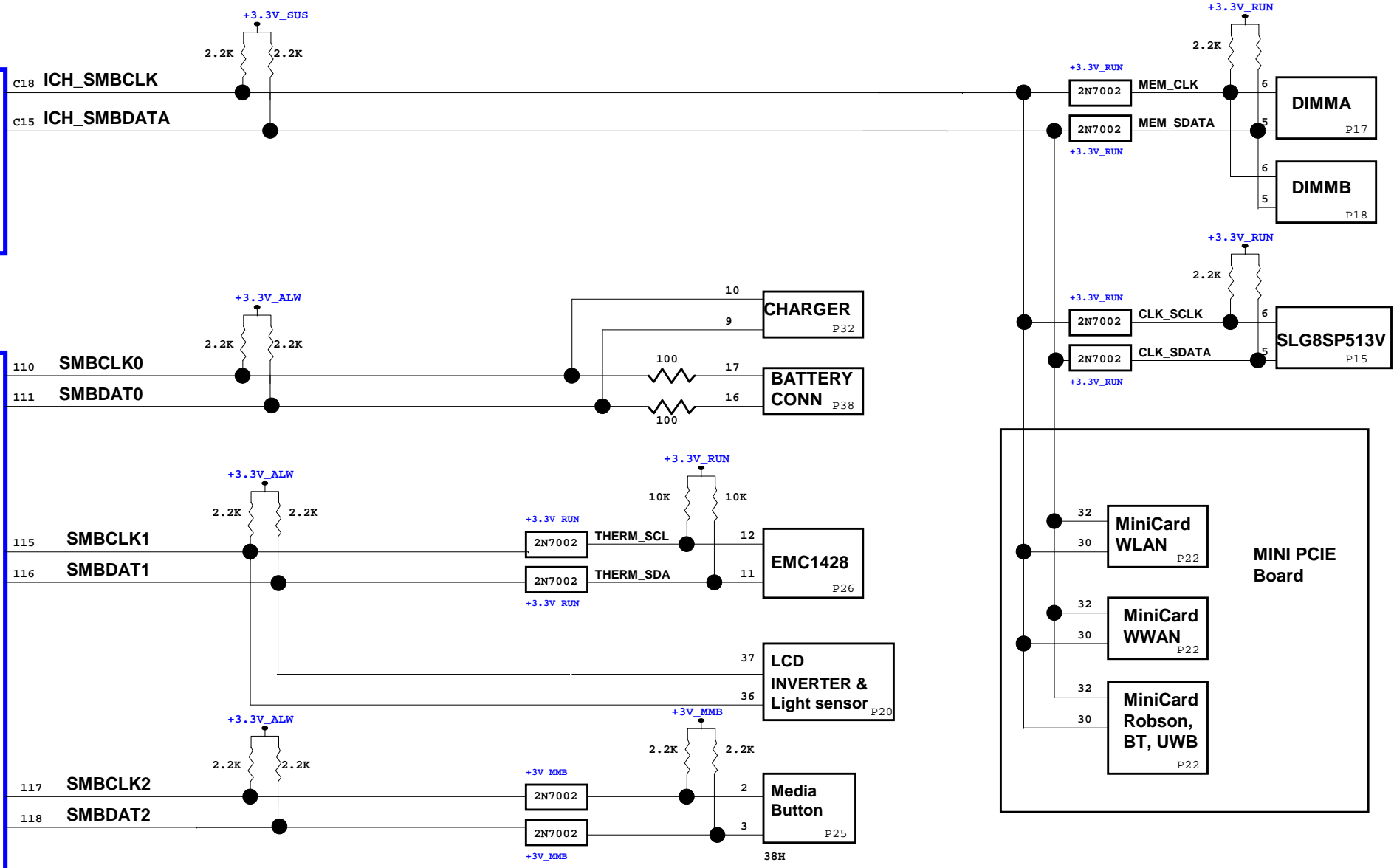
QUANTA
COMPUTER

Title		
SCREW PAD		
Size	Document Number	Rev
	SS5	1A
Date:	Thursday, January 08, 2009	Sheet 39 of 44

Reserved for EMI. stitching caps.


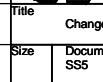


Title					EMI CAP				
Size	Document Number								Rev
	SS5								1A
Date:	Thursday, January 08, 2009				Sheet	40	of	44	




Change List						
Item	Page#	Date	T	Issue Description	Solution Description	Rev
				X00 change to X00.1		
1	12	5/20/2008	EE	Schematic have pull up resistor and pull down resistor. Remove all pull up resistor for those signal. SB_WWAN_PCIE_RST#, SB_LOM_PCIE_RST#, SB_WPAN_PCIE_RST#, SB_WLAN_PCIE_RST# and SB_NB_PCIE_RST#.	Depop R361, R133, R72, R407, R74.	X00.1
2	20, 28	5/20/2008	EE	LCD and CCD connect need combin as one connect. Del Camera connect (P28) and change (P20)J1 from 30pin to 44pin. Move 2 USB and 1 Combo connect to MB.	Del CON12(P28) and move rest of Camera componets to P20. Change J1 from 30pin to 44pin.	X00.1
3	23	5/20/2008	EE	Move IO Board connect (2 USB and 1 E-Sata) to Mother Board side.	Add L38, R468, R469, CN1 For USB0 Add L39, R470, R471, CN2 and ESD1 for USB1. Add L40, R472, R473, CON20 for USB2 & E-SATA	X00.1
4	23	5/20/2008	EE	To support USB charger function, Added USB Switch to solve leakage issue.	Added U46 and R474 USB Switch circuit.	X00.1
5	23	5/20/2008	EE	Follow safety design, added Fuse on USB power avoide TPS2062DR no function.	Added PJP9 and FS1_NC for USB0 and USB1. Added PJP10 and FS2_NC for USB3.	X00.1
6	3, 26	5/20/2008	EE	Follow Thermal requirement to measured OTP, CPU, NB, DDR, SB and WWAN temperature.	Added C501, C502, Q48, C503, Q49 for DDR and NB. Added C504, C505, Q50, C506, Q51 for SB and WWAN Added rest of EMC1428 components C508, R477, R475, R476	X00.1
7	12, 23	5/20/2008	EE	For USB P0/P1 use same power rail. Change over current design. Change net OC0# and OC1# to OC0_1#.	Change U17.5 and U17.8 to net OC0_1#. Remove R132.	X00.1
8	25	5/21/2008	EE	Change MMB connect from 15pin to 10pin. Remove Media Buttom function. Added System LED signal on MMB connect.	Change CON11 from 15pin to 10pin. Added SYS_WHITE#_R and SYS_AMBER#_R signal MMB connect.	X00.1
9	28	5/21/2008	EE	Follow ME/ID requirement. Change Audio connect type.	Udate CON2 symbol and footprint.	X00.1
10	38	5/21/2008	EE	Follow ME/ID requirement. Change DC_IN Jack connect type.	Udate CON6 symbol and footprint.	X00.1
11	11	5/23/2008	EE	ME Z-Hing limite, need change RTC type to small size. It need support charge function.	Chnge CON1 footprint and Added R202 1kohm support charge.	X00.1
12	13, 22	5/23/2008	EE	Added USB_MCARD3 detect pin for WWAN card.	Added input port on USSB_MCARD3 and connect to CON15.21	X00.1
13	18	5/23/2008	EE	Memory A and B chanel have same SMBUS address. Change SMBUS address to A4.	Change R147 from pull low to pull up +3.3V_RUN.	X00.1
14	19	5/23/2008	EE	Display Port need chnge to TOP mount type. Change new Connect Footprint.	Change CON7 symbol and Footprint.	X00.1
15	20, 21	5/23/2009	EE	Added SMBUS signal and connection to LCD Connect(J1).	Added SMB_CLK1 form U35.115 to J1.6. SMB_DAT1 from U35.116 to J1.5.	X00.1
16	21, 31	5/23/2009	EE	Remove GPIO diode on GPD0, GPF1 and GPF2.	GPFO -> SIO_SLP_S3# solve S5 can enter issue. (Remove D0) GPF1 -> IMVP_PWRGD input pin, can't havd diode. (Remove D17) GPF2 -> RESET_OUT# out put pin, don't have leakage concern. (Remove D7 and R110)	X00.1
17	22, 27	5/23/2009	EE	ME define MIC connect on MB side.Remove MIC signal to 100 pin connect. Change those 2 pin for Thermal Diode signal(WWAN).	REM_DIODE6P_7N -> CON15.98 connection to U43.15 REM_DIODE6N_7P -> CON15.99 connection to U43.14	X00.1
18	22	5/23/2009	EE	ID don't support WLAN/WWAN/WPAN LED. Remove LED signal from CON15. Added 1 pin +5VRUN.	Remove out LED_WWAN#/ LED_BT_UWB# / LED_WLAN_OUT#. CON15-21,56 and 87pin	X00.1
19	23	5/23/2009	EE	Change USB connect layout footprint.	Change CN1 schematic symbol and layout footprint. Change CN2 schematic symbol and layout footprint.	X00.1
20	23	5/23/2009	EE	Change E-Sata/USB connect layout footprint. Added detect# signal for detect USB plug in.	Change CON20 E-Sata/USB connect layout footprint. Connection CON20.14 (USB_COM_DETECT#) to EC.	X00.1
21	24	5/23/2009	EE	Sync with ME and EE keyboard Matrix. Update Footprint.	Update CON19 layout footprint and reserve keyboard pin to match M09 keyboard.	X00.1
22	25	5/23/2009	EE	Power LED and System LED need light during S5. Due to S5 state, +5V-ALW will turn off.	Change R431, U42.5, R393, U33.5, R330, U29.5, R404, U40.5 from +5V_ALW to +5V_ALW2.	X00.1
23	21	5/23/2009	EE	Move Back R233 to MB. Reserved GPIO pull up for EC WUI pin.	Move R233 pull up (+3.3V_ALW) to U35.124 Media_INT#.	X00.1
24	9	5/23/2009	EE	Follow Intel Reference Design. Added AC terminal RC.	Added R479 (0.51ohm) and C502 (22uF) on +1.05M_MPLL	X00.1
25	27	5/23/2009	EE	Add R480 100k on 92HD73C pin 13 SENSEA.	Add R480 100k on 92HD73C pin 13 SENSEA.	X00.1
26	32	5/23/2009	P	Change ACIN threshole to 11.9V from 17V	Change PR116 from 365K/F ohm to 240K/F ohm.	X00.1
27	38	5/23/2009	P	Change to +5V_ALW from +5V_ALW2.	Chanage PR3 pin1 to +5V_ALW from +5V_ALW2.	X00.1
28	38	5/26/2009	P	Change CON17 to FLS030HP1 and update footprint.	Change CON17 footprint to fl4sxxxhp1-30p-r	X00.1
29	38	5/26/2009	EE	Follow layout request to exchange signals.	Exchange CP0, CP2, CP3, CP4, CP5, L18 signals for layout request.	X00.1
30	29	5/28/2009	EE	Follow BCM recommand. Change Pin 27 to correct power rail and add 0.1uF*4 for π type filter.	Change U21.27 to U21.30 and Add C509~C512 at +1.2V_LOM.	X00.1
31	9	5/29/2009	EE	Depop R118 to let VCC_HDA connect to GND.	Depop R118 0 ohm.	X00.1
32	25	5/29/2009		The different power rail between MMB and SIO. Need added level circuit.	Added Q48, Q53, Q52, RP22level shift circuit.	X00.1
PROJECT : SS5		DOC. NO. : 204		REV: X00		
APPROVED BY : Cory Lin		CHECKED BY: Cory Lin		DRAWN BY : Leo Tseng	DATE : May. 19, 2008	SHEET 9 OF 11
				QUANTA COMPUTER		
				QUANTA COMPUTER		
				Rev 1A		
				Sheet 42 of 44		

Change List

Item	Page#	Date	T	Issue Description	Solution Description	Rev
				X00.1 change to X01		
33	32	6/10/2008	EE	Change AC_IN volt threshold on 13.5V with a 280K resister of PR116	Change PR116 from 240K to 280K	X01
34	32	6/11/2008	EE	Change to SI7326 for 2.2A charging	Change PQ24 from SI7114DN to SI7326DN	X01
35	32	6/11/2008	EE	No need to populate them	unpop PR1 and PC0	X01
36	35	6/11/2008	EE	Adjust the slew rate of load line	Chagne PR93 and PR66 from 3.83K to 11.8K Chagne PR104 from 1K to 4.99K, PR108 from 3.83K to 6.49K Chagne PC18 from 0.22u to 0.033u, PC21 from 0.022u to 3300P	X01
37	32-36	6/11/2008	EE	Replace 0R/0603 resister by power jumper	Chagne 0R/0603 to power jumper as the SJ1, SJ2, , SJ3, SJ4	X01
38	32-36	6/11/2008	EE	Replace 0R/0606 resister by short	Replace 0R/0606 resister by short as the PR102, PR103, PR59 , PR68	X01
39	34	6/11/2008	EE	Adjust controller Freq on 400K/300K from 200K/300K	PR32 NC and pop PR33	X01
40	20	6/11/2008	EE	Follow ME define Camera routing. Added Camera connect.	Added CON12 camera connect.	X01
41	19	6/11/2008	EE	DVI monitor can not detected by DVI dongle.	Follow Intel reference Board, added MUX to select I2C or AUX signal.	X01
42	3	6/16/2008	EE	Move CPU ITP Debug test pad to bottom side for ICT engineer requirement.	Added T113, T114, T115, T116 and T117 put on Bottom side.	X01
43	6	6/16/2008	EE	Added NB JTAG Debug test pad on bottom side for ICT engineer requirement.	Added T118, T119, T120 and T121 put on Bottom side.	X01
44	8	6/16/2008	EE	Modify +VDD_GFXCORE power enable pin follow intel CRB design.	Added R485, Q55 and R486.	X01
45	21	6/16/2008	EE	Follow Quanta M09 lesson learn. Connect HD_RST# signal to EC for Mute timing control.	Added ICH_AZ_CODEC_RST# connect to SIO(U35.22)	X01
46	21,24	6/22/2008	EE	Follow MRD design added CAP LED circuit.	ITE8512 (U35.88) GPIO for Cap_LED#. Added R453, R450, Q56, Q59 and R446.	X01
47	24	6/22/2008	EE	Change LED_KB circuit. Change to PWM control.	Modify Q39.	X01
48	31	6/22/2008	EE	Solve Bits issue DF225364, CMOS load defalut when disconnect AC.	Added Pull down on RESET_OUT# to avoid ICH_PWRGD glitch in inital state.	X01
49	3	6/22/2008	EE	H_RESET leakage from pull up resisrtor. Follow Intel remove out it.	Depop R300.	X01
50	3	6/24/2008	EE	+3.3V_RUN faster then H_THERM. H_THERMTRIP will cause +3.3V_ALW shut down.	Change R204 to form 1M to 10M. It will delay Q17 turn on timing.	X01
51	21	6/24/2008	EE	SIO_SLP_S3# have glitch from EC when system power up. Add PD resistor to solve it.	Pull down R487 1k ohm at SIO_SLP_S3#.	X01
52	8	6/24/2008	EE	GFX_VR_EN(0.9V) can't meet 2N7002W-7-F(Vgs=1V~2V). Need change to FDV301N(Vgs=0.85V).	Chagne Q55 from 2N7002W-7-F to FDV301N.	X01
53	29	6/25/2008	EE	Follow Crystal test report. Chagne LAN Crystal caps from 22pF to 33pF.	Chagne C272, C305 from 22pF to 33pF.	X01
54	21	6/25/2008	EE	Reserve PLTRST# option at for U35 pin 20 to detect SIO_A20.	Add R488, R489 to option ICH_PME#, PLTRST#.	X01
55	28	6/25/2008	EE	Follow IDT feedback. Change L3, L5 to BLM18BD601SN1D for AP test.	Change L3, L5 to BLM18BD601SN1D.	X01
56	40	6/25/2008	EE	Follow EMI team feedback. Reserve spring for EMI.	Add PV1~PV10.	X01
57	23	6/25/2008	EE	Follow EMI team feedback. Connect USB connecot dip pin to GND.	Connect CN1, CN2 pin 7, 8 to GND.	X01
58	3	6/26/2008	EE	Reserve R490 1M ohm for Q17 compatible FDV301V.	Add R490 1M ohm and pull up +V1.05S_CPU.	
				X01 change to X02		
1	27	7/22/2008	EE	Change port F to port A for Microsoft default drive support port A only.	Change port F to port A also swap SENSEA, SENSEB circuit.	X02
2	3,5,6,8,11,13 20,21,28,29,31	8/13/2008	EE	Remove 0 ohm.	Remove R173, R430, R354, R239, R282, R405, R178, R243, R244, R277, R47, R488, R132, R203, R152, R153, R311, R16, R19, R30	X02
3	6,9,13,17,18,21 27,29,34,35	8/14/2008	EE	Remove 0 ohm.	R134, R435, R448, R70, R199, R394, PR58, R161, R319, R260, R261, R353, R357, R313, R329, PR56, R61, R322, R323, R335, R337, R383, R106, R43, PR98	X02
4	23	8/15/2008	EE	Change USB choke to DLP11SN900HL2L for Z-high form 1.6mm to 0.6mm.	Change L38, L39, L40 fp and remove R468, R469, R470, R471, R472, R473.	X02
5	26	8/28/2008	EE	System can't shut down during OTP sest to 85 degree C.Follow SDA to modify OTP to 83 degree C.	Change R477 from 562 ohm to 487 ohm.	X02
6	11	8/29/2008	EE	Confirm Safty team to depop D10 and R136 for RTC charge function.	Depop D10 and R136 10k ohm.	X02
7	35	9/3/2008	EE	Changes for cost down (CPU regulator from two to one phase)	Depop PC53, PR67, PR73, FL3, PC100, PC101, PC93, PC97, PC1, PR107, PC92, PQ3, PQ2, PR106, PC94, PL1, PC95, PC3, PR93, PR90, PR101, PR95, PC77, PR88, PC86, PC85, and PR96 Change PR66 from 11.8K to 1.8K, PR104 from 4.99K to 4.02K, PR108 from 6.49K to 1.8K, PC21 from 3300P to 0.01u, PC18 from 0.033 to 0.068, PR81 from 12.7K to 20K, PR87 from 6.81K to 4.99K, PR91 from 1K to 2K Add a resister of PR20(0R)	X02
8	33, 36, 37	9/3/2008	EE	Changes for cost down	Depop PC25, PC105, PC110, PC39 and PC40 Change PQ23 from SI7326DN to SI3424DV, PQ20 from SI7326DN to SI3424DV, PQ22 from SI7114DN to SI7326DN,	X02
					 QUANTA COMPUTER	
PROJECT : SS5			DOC. NO. : 204		REV: X00	
APPROVED BY : Cory Lin			CHECKED BY: Cory Lin		DRAWN BY : Leo Tseng	DATE : May. 19 , 2008
					SHEET 9 OF 11	
					 QUANTA COMPUTER	Rev 1A
					Date: Thursday, January 08, 2009	Sheet 43 of 44

Change List

Item	Page#	Date	T	Issue Description	Solution Description	Rev
9	38	9/3/2008	PR	Reserve a protection circuit to avoid vottage variation of input (13<Vin<20)	Add some parts of PR492, Pr493, PR491, PD35, PD36, PQ51, PQ61 and PQ62	X02
10	21	9/4/2008	EE	H/W workaround for DOS re-boot commend.	Depop R489 and Pop R488 0 ohm resistor.	X02
11	6, 8, 20, 21	9/4/2008	EE	Remove R250, R467, R157 0 ohm.	Remove R250, R467, R157 0 ohm.	X02
12	22	9/8/2008	EE	Reserve DMIC DATA/CLK to Minipcie board.	Reserve DMIC DATA/CLK to CON15 pin 56, 93	X02
13	33	9/8/2008	EE	Short PJP6 for thermal module have latch in Power jump.	Remove PJP6 and change +1.8V_RUN_P to +1.8V_SUS.	X02
14	18	9/8/2008	EE	Add C515 for memory +1.5V_MD.	Add C515 for memory +1.5V_MD.	X02
15	23	9/8/2008	EE	To fix USB charge on Blackberry and Ipod in S5 issue.	Change U46 to MAX4983E. Add R491, R492, R493, R494, C516, R495, R496, R497. Remove ESD2.	X02
16	20	9/15/2008	EE	Supply DPST function	Depop R270 and Pop R271 resistor.	X02
17	21	9/15/2008	EE	For cost down ,remove debug LED	Depop R83,R112,R198,LED0,LED1,LED2	X02
				X02 change to X02.1		
18	38	9/18/2008	EE	For Safty to add fuse at battery connector.	Add FS3 at CON17	X02.1
19	6, 21	9/26/2008	EE	Add L_BKLT_EN connect NB's L_BKLT_EN and EC pin 48 to slove LCD can't dispaly issue.	Add L_BKLT_EN connect U6 pin C37 to EC pin 48.	X02.1
20	17, 18	10/02/2008	EE	Follow Intel feedback. Each DRAM device needs to have its own ZQ cal resistor.	Add R498~R505 240 ohm to DRAM U23, U24, U25, U26, U36, U37, U38, U39.	X02.1
21	21	10/07/2008	EE	Change BID from X02 to X02.1	Depop R102, R100, R126 and pop R109, R126, R127 100k ohm.	X02.1
22	13	10/07/2008	EE	Re-add ICH_SMLINK0/1 PU resistor and reserve R260, R261.	Reserve and depop R260, R261 0 ohm and Add RP8 PU resistor for ICH_SMLINK0/1.	X02.1
23	38	10/08/2008	EE	Confirm Power team to remove fuse. fuse move on battery.	Rmove FS3 and short by shape.	X02.1
24	33	10/16/2008	PR	rise center voltage from 1.79V to 1.82V	change PR36 from 12.4KF to 15.8KF, and PR35 from 10KF to 12.4K, and pop PC39	X02.1
25	35	10/16/2008	PR	PL2 is not in PSL, so channg it to Toko which is in PSL. And adjust some values for PL2's change.	change PR92 from 97.6K to 200K, PR91 from 2K to 499R, PR104 from 4.02K to 2K, PR108 from 1.8K to 2.61K, PC21 from 0.01uF to 0.1uF, PC18 from 0.068uF to 0.022uF, pop PC3	X02.1
				X02.1 change to A00		
1	27	11/10/2008	EE	Change TPA6040A4 GAIN from 15.6dB to 6dB for speaker midified.	Depop R296 and pop R295 100k ohm.	A00
2	21	11/10/2008	EE	Change Board ID to A00.	Depop R217 and pop R100 10k ohm.	A00
3	3, 34	11/10/2008	EE	Remove PJP0, PJP2 and short by trace for 1.05V, 1.5V.	Remove PJP0, PJP2 and short by trace for 1.05V, 1.5V.	A00
4	36	11/10/2008	EE	Remove PJP1, PJP3 and short by trace for 3.3V, 5V.	Remove PJP1, PJP3 and short by trace for 3.3V, 5V.	A00
5	34, 36	11/10/2008	EE	Remove PJP4, PJP5 and short by trace for +PWR_SRC.	Remove PJP4, PJP5 and short by trace for +PWR_SRC.	A00
6	33	11/10/2008	EE	Remove PJP8 and short by trace. Change PU4.1, PU4.2 to +1.5V_MEM.	Remove PJP8 and short by trace. Change PU4.1, PU4.2 to +1.5V_MEM.	A00
7	36	12/22/2008	EE	Rising up OCP point to cover second source controller IC of PU0	Change PR11 from 110k ohm to 147k ohm.	A00
8	33	12/22/2008	EE	Remove R451 0 ohm and short by trace. Change 0.75V_P to for +0.75V_DDR_VTT.	Remove R451 0 ohm and short by trace. Change 0.75V_P to for +0.75V_DDR_VTT.	A00
9	33	12/29/2008	EE	Remove R451 will effect DDR reference voltage trace.	Restore the R451 0 ohm.	A00
10	33, 34	12/29/2008	P	Remove PR118, PR117 0 ohm and short by trace. Change S5_1.8V to SUS_ON, S3_1.8V to RUN_ON.	Remove PR118, PR117 0 ohm and short by trace. Change S5_1.8V to SUS_ON, S3_1.8V to RUN_ON.	A00
11	33	12/29/2008	P	Remove PR29 0 ohm and short by trace. Remove PR30 *0_NC and NC.	Remove PR29 0 ohm and short by trace. Remove PR30 *0_NC and NC.	A00
12	34	12/29/2008	P	Remove PR34, PR47, PR49, PR55 0 ohm and short by trace. Change EN_2 to RUN_ON.	Remove PR34, PR47, PR49, PR55 0 ohm and short by trace. Change EN_2 to RUN_ON.	A00
13	34	12/29/2008	P	Remove PR33 0 ohm and short by trace. Remove PR32, PR37 *0_NC and NC.	Remove PR33 0 ohm and short by trace. Remove PR32, PR37 *0_NC and NC.	A00
14	36	12/29/2008	P	Remove PR85, PR83, PR12 0 ohm and short by trace. Remove PR10 *0_NC and NC.	Remove PR85, PR83, PR12 0 ohm and short by trace. Remove PR10 *0_NC and NC.	A00
15	36	12/29/2008	P	Remove PR13, PR17 0 ohm and short by trace. Remove PR16 *0_NC and NC.	Remove PR13, PR17 0 ohm and short by trace. Remove PR16 *0_NC and NC.	A00
16	36	12/29/2008	P	Remove PR9 0 ohm and short by trace. Remove PR6, PR7 *0_NC and NC.	Remove PR9 0 ohm and short by trace. Remove PR6, PR7 *0_NC and NC.	A00
17	36	12/29/2008	P	Change PR79, PR80 to short jump SJ5, SJ6.	Change PR79, PR80 to short jump SJ5, SJ6.	A00
18	25	12/29/2008	EE	Change Power/System LED resistor from 220 to 1k ohm to reduce LED brightness.	Change R360 , R382, R366, R442 from 220 to 1k ohm.	A00
19	27	12/29/2008	EE	Follow Dell request. Change TPA6040A4 GAIN from 6dB to 10dB for speaker midified.	Depop R168 and pop R167 100k ohm.	A00
20	9, 14, 27	01/05/2009	EE	Change GMH, ICH, IDT HDA power to 1.5V for slove HDMI no sound issue.	Depop R117 and pop R118 0 ohm. Change U41.3, R101.1 to +1.5V_RUN and R120.1 to +V1.5_MD.	A00
21	21	01/06/2009	EE	HDA bus are +1.5V power rail. The ICH_AZ_CODEC_RST# also need add level shift to connect EC.	Add R506 100k ohm , R507 390k ohm, C135 0.1uF, Q60 3904, Q61 2N7002.	A00
22	20	02/05/2009	EE	Add DPST fntion in ST build.	Depop R271 10k ohm and pop R269 0 ohm.	A00
23	21	02/05/2009	EE	Remove C135 to reduce Q60 pin 2 rise time. It will effect ICH_AZ_CODEC_RST2# asserted.	Depop C135 0.1uF.	A00
24	27	02/05/2009	EE	Follow Speaker Vendor NXP to moidfy AMP caps.	Change C33, C34 from 0.033U to 0.0047U and C140, C149 from 0.033U to 0.0047U.	A00
25	19	02/05/2009	EE	Diode causing voltage drop. The VGA controller on the dongle goes into reset and stops functioning	Change D14 Diode to Fuse 0805L100WR and there is no voltage drop on VGA controller.	A00
26	20	02/23/2009	EE	LCD self test function lose (D + Power Button) when enable DPST function.	Pop R270 0 ohm and change R260 to 100 ohm.	
PROJECT : SS5				DOC. NO. : 204	REV: A00	<div><div>QUANTA COMPUTER</div></div> <div>TitleChange List1QUANTA</div> <div>SizeDocument NumberSS5Rev1A</div> <div>Date:Monday, February 23, 2009Sheet44 of 44</div>
APPROVED BY : Cory Lin				CHECKED BY: Cory Lin	DRAWN BY : Leo Tseng	
				DATE : May. 19, 2008	SHEET 9 OF 11	